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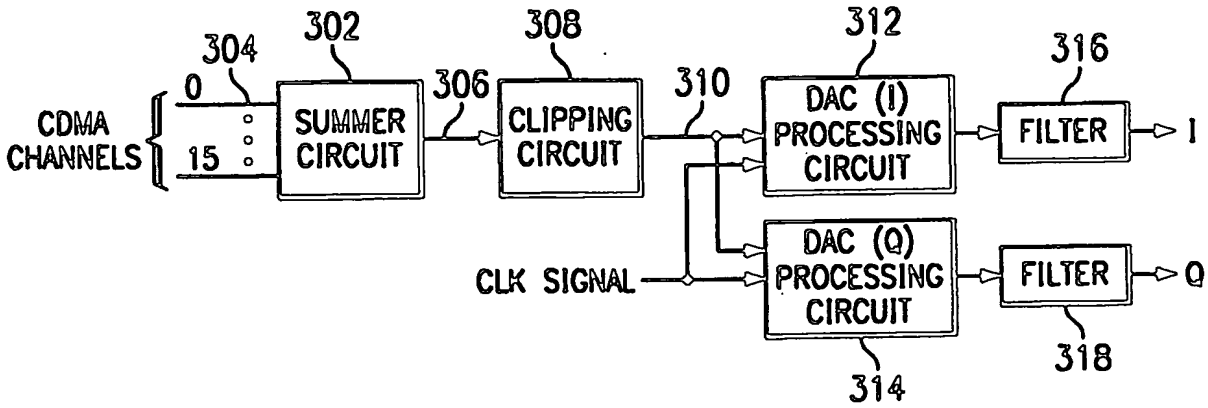

(57) Abstract

A CDMA signal processing circuit (300) includes a summer circuit (302) that receives a plurality of CDMA signals from a plurality of channels (304). The summer circuit (302) combines the plurality of CDMA signals according to a power magnitude value and power direction value associated with each CDMA signal. The summer circuit (302) generates a summed signal (306) that is applied to a clipping circuit (308). The clipping circuit (308) removes a portion of the summed signal (306) outside a desired threshold range and generates a clipped signal (310) therefrom. Digital to analog processing circuits (312 and 314) convert the clipped signal (310) into a half width encoded format. Digital to analog processing circuits (312 and 314) transform the half width encoded clipped signal into analog I and Q signals, respectively. The analog I and Q signals are applied to corresponding filters (316 and 318) prior to transmission.

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CDMA TRANSMISSION EMPLOYING CLIPPING FUNCTION

TECHNICAL FIELD OF THE INVENTION

The present invention relates in general to signal processing techniques and more particularly to an apparatus and method of processing CDMA signals.

BACKGROUND OF THE INVENTION

The use of code division multiple access (CDMA) signals is a convenient technique of transmitting wireless signals. Many wireless systems process CDMA signals for the transmission of information. However, typical CDMA signal processing techniques suffer inefficient power in the desired band of frequencies for transmitted signals and unacceptable intersymbol interference. Therefore, it is desirable to increase frequency band power and reduce intersymbol interference.

SUMMARY OF THE INVENTION

From the foregoing, a need has arisen for processing CDMA signals to increase frequency band power. A need has also arisen for processing CDMA signals to reduce intersymbol interference.

An object of the invention is to provide an apparatus and method of processing CDMA signals that substantially eliminate or reduce disadvantages and problems associated with conventional CDMA processing techniques.

In accordance with one aspect of the invention, there is provided a method of processing CDMA signals, comprising the steps of:

performing a spreading function on CDMA signals from a plurality of channels;

combining the CDMA signals of the plurality of channels to create a summed signal;

removing a portion of the summed signal above and below a desired threshold range to create a clipped signal.

In accordance with another aspect of the invention, there is provided a method of processing CDMA signals, comprising the steps of:

performing a spreading function on CDMA signals from a plurality of channels;

combining the CDMA signals of the plurality of channels to create a summed signal;

converting the summed signal into two separate data channels for modulating a radio frequency carrier transmission signal, each of the two separate data channels carrying information in a half-width pulse configuration, wherein a first half of the pulse contains valid information and a second half of the pulse has a return to zero format.

In accordance with a further aspect of the invention, there is provided an apparatus for processing CDMA signals, comprising:

a summer circuit operable to combine CDMA signals from a plurality of channels, the summer circuit operable to generate a summed signal therefrom;

a clipping circuit operable to remove a portion of the summed signal above and below a desired threshold range, the clipping circuit operable to generate a clipped signal therefrom;

a digital to analog processing circuit operable to convert the clipped signal into a half width encoded format, the half width encoded format having information contained in a first half of a signal pulse and no information in a second half of the signal pulse, the digital to analog processing circuit operable to convert the clipped signal in the half width encoded format to an analog signal;

a filter operable to reduce inter-symbol interference in the analog signal.

According to an embodiment of the present invention, a method of processing CDMA signals includes performing a spreading function on CDMA signals from a plurality of channels. The CDMA signals from the plurality of channels are combined to create a summed signal. A portion of the summed signal above and below a desired threshold range is removed to create a clipped output signal.

The present invention provides various technical advantages over conventional CDMA processing techniques. For example, one technical advantage is to clip CDMA signals from multiple channels to improve handling of more frequently occurring values falling within the desired clipping region. Another technical advantage is to effectively filter clipped CDMA to reduce intersymbol

interference. Yet another technical advantage is to encode clipped CDMA signals into a half width format for increased power in a desired band of frequencies. Other technical advantages are readily ascertainable to one skilled in the art from the following figures, description, and claims.

BRIEF DESCRIPTION OF THE DRAWINGS

An embodiment of the invention will be described hereinafter, by way of example only, with reference to the accompanying drawings in which like reference signs are used for like features and in which:

Figure 1 is a schematic overview of an example of a wireless telecommunications system in which an example of the present invention is included;

Figure 2 is a schematic illustration of an example of a subscriber terminal of the telecommunications system of Figure 1;

Figure 3 is a schematic illustration of an example of a central terminal of the telecommunications system of Figure 1;

Figure 3A is a schematic illustration of a modem shelf of a central terminal of the telecommunications system of Figure 1;

Figure 4 is an illustration of an example of a frequency plan for the telecommunications system of Figure 1;

Figures 5A and 5B are schematic diagrams illustrating possible configurations for cells for the telecommunications system of Figure 1;

Figure 6 is a schematic diagram illustrating aspects of a code division multiplex system for the telecommunications system of Figure 1;

Figure 7 is a schematic diagram illustrating signal transmission processing stages for the telecommunications system of Figure 1;

Figure 8 is a schematic diagram illustrating signal reception processing stages for the telecommunications system of Figure 1;

Figure 9 is a schematic diagram illustrating downlink and uplink communication paths for the wireless telecommunications system;

Figure 10 is a schematic diagram illustrating the makeup of a downlink signal transmitted by the central terminal;

Figure 11 is a graphical depiction illustrating the phase adjustment to a slave code sequence of the subscriber terminal;

Figure 12 is a graphical depiction of a signal quality estimate performed by the receiver in the subscriber terminal;

Figure 13 is a graphical diagram illustrating the contents of a frame information signal within the downlink signal;

Figure 14 is a tabular depiction illustrating overhead insertion into a data stream of the downlink signal;

Figure 15 is a tabular depiction of a power control signal in an overhead channel of the downlink signal;

Figure 16 is a tabular depiction of a code synchronization signal in the overhead channel of the downlink signal;

Figure 17 is a graphical depiction of a transmitting power and a transmit rate for each mode of operation of the wireless telecommunications system;

Figure 18 is a schematic diagram illustrating the operation of the receiver and transmitter in the subscriber terminal;

FIGURE 19 illustrates a simplified schematic diagram of a CDMA signal processing circuit;

FIGURE 20 illustrates a clipping operation performed by the CDMA signal processing circuit;

FIGURE 21 illustrates a half width encoding operation performed by the CDMA signal processing circuit; and

FIGURE 22 illustrates a filtering operation performed by the CDMA signal processing circuit.

DETAILED DESCRIPTION OF THE INVENTION

Figure 1 is a schematic overview of an example of a wireless telecommunications system. The telecommunications system includes one or more service areas 12, 14 and 16, each of which is served by a respective central terminal (CT) 10 which establishes a radio link with subscriber terminals (ST) 20 within the area concerned. The area which is covered by a central terminal 10 can vary. For example, in a rural area with a low density of subscribers, a service area 12 could cover an area with a radius of 15-20Km. A service area 14 in an urban environment where is there is a high density of subscriber terminals 20 might only cover an area with a radius of the order of 100m. In a suburban area with an intermediate density of subscriber terminals, a service area 16 might cover an area with a radius of the order of 1Km. It will be appreciated that the area covered by a particular central terminal 10 can be chosen to suit the local requirements of expected or actual subscriber density, local geographic considerations, etc, and is not limited to the examples illustrated in Figure 1. Moreover, the coverage need not be, and typically will not be circular in extent due to antenna design considerations, geographical factors, buildings and so on, which will affect the distribution of transmitted signals.

The central terminals 10 for respective service areas 12, 14, 16 can be connected to each other by means of links 13, 15 and 17 which interface, for example, with a public switched telephone network (PSTN) 18. The links can include conventional telecommunications technology using copper wires, optical fibres, satellites, microwaves, etc.

The wireless telecommunications system of Figure 1 is based on providing fixed microwave links between subscriber terminals 20 at fixed locations within a service area (e.g., 12, 14, 16) and the central terminal 10 for that

service area. In a preferred embodiment each subscriber terminal 20 is provided with a permanent fixed access link to its central terminal 10. However, in alternative embodiments demand-based access could be provided, so that the number of subscribers which can be serviced exceeds the number of telecommunications links which can currently be active.

Figure 2 illustrates an example of a configuration for a subscriber terminal 20 for the telecommunications system of Figure 1. Figure 2 includes a schematic representation of customer premises 22. A customer radio unit (CRU) 24 is mounted on the customer's premises. The customer radio unit 24 includes a flat panel antenna or the like 23. The customer radio unit is mounted at a location on the customer's premises, or on a mast, etc., and in an orientation such that the flat panel antenna 23 within the customer radio unit 24 faces in the direction 26 of the central terminal 10 for the service area in which the customer radio unit 24 is located.

The customer radio unit 24 is connected via a drop line 28 to a power supply unit (PSU) 30 within the customer's premises. The power supply unit 30 is connected to the local power supply for providing power to the customer radio unit 24 and a network terminal unit (NTU) 32. The customer radio unit 24 is also connected to via the power supply unit 30 to the network terminal unit 32, which in turn is connected to telecommunications equipment in the customer's premises, for example to one or more telephones 34, facsimile machines 36 and computers 38. The telecommunications equipment is represented as being within a single customer's premises. However, this need not be the case, as the subscriber terminal 20 preferably supports either a single or a dual line, so that two subscriber lines could be supported by a single subscriber terminal

20. The subscriber terminal 20 can also be arranged to support analogue and digital telecommunications, for example analogue communications at 16, 32 or 64kbits/sec or digital communications in accordance with the ISDN BRA standard.

Figure 3 is a schematic illustration of an example of a central terminal of the telecommunications system of Figure 1. The common equipment rack 40 comprises a number of equipment shelves 42, 44, 46, including a RF Combiner and power amp shelf (RFC) 42, a Power Supply shelf (PS) 44 and a number of (in this example four) Modem Shelves (MS) 46. The RF combiner shelf 42 allows the four modem shelves 46 to operate in parallel. It combines and amplifies the power of four transmit signals, each from a respective one of the four modem shelves, and amplifies and splits received signals four way so that separate signals may be passed to the respective modem shelves. The power supply shelf 44 provides a connection to the local power supply and fusing for the various components in the common equipment rack 40. A bidirectional connection extends between the RF combiner shelf 42 and the main central terminal antenna 52, typically an omnidirectional antenna, mounted on a central terminal mast 50.

This example of a central terminal 10 is connected via a point-to-point microwave link to a location where an interface to the public switched telephone network 18, shown schematically in Figure 1, is made. As mentioned above, other types of connections (e.g., copper wires or optical fibres) can be used to link the central terminal 10 to the public switched telephone network 18. In this example the modem shelves are connected via lines 47 to a microwave terminal (MT) 48. A microwave link 49 extends from the microwave terminal 48 to a point-to-point

microwave antenna 54 mounted on the mast 50 for a host connection to the public switched telephone network 18.

A personal computer, workstation or the like can be provided as a site controller (SC) 56 for supporting the central terminal 10. The site controller 56 can be connected to each modem shelf of the central terminal 10 via, for example, RS232 connections 55. The site controller 56 can then provide support functions such as the localization of faults, alarms and status and the configuring of the central terminal 10. A site controller 56 will typically support a single central terminal 10, although a plurality of site controllers 56 could be networked for supporting a plurality of central terminals 10.

As an alternative to the RS232 connections 55, which extend to a site controller 56, data connections such as an X.25 links 57 (shown with dashed lines in Figure 3) could instead be provided from a pad 228 to a switching node 60 of an element manager (EM) 58. An element manager 58 can support a number of distributed central terminals 10 connected by respective connections to the switching node 60. The element manager 58 enables a potentially large number (e.g., up to, or more than 1000) of central terminals 10 to be integrated into a management network. The element manager 58 is based around a powerful workstation 62 and can include a number of computer terminals 64 for network engineers and control personnel.

Figure 3A illustrates various parts of a modem shelf 46. A transmit/receive RF unit (RFU - for example implemented on a card in the modem shelf) 66 generates the modulated transmit RF signals at medium power levels and recovers and amplifies the baseband RF signals for the subscriber terminals. The RF unit 66 is connected to an analogue card (AN) 68 which performs A-D/D-A conversions,

baseband filtering and the vector summation of 15 transmitted signals from the modem cards (MCs) 70. The analogue unit 68 is connected to a number of (typically 1-8) modem cards 70. The modem cards perform the baseband signal processing of the transmit and receive signals to/from the subscriber terminals 20. This includes 1/2 rate convolution coding and x 16 spreading with CDMA codes on the transmit signals, and synchronization recovery, de-spreading and error correction on the receive signals. Each modem card 70 in the present example has two modems, each modem supporting one subscriber link (or two lines) to a subscriber terminal 20. Thus, with two modems per card and 8 modems per modem shelf, each modem shelf could support 16 possible subscriber links. However, in order to incorporate redundancy so that a modem may be substituted in a subscriber link when a fault occurs, only up to 15 subscriber links are preferably supported by a single modem shelf 46. The 16th modem is then used as a spare which can be switched in if a failure of one of the other 15 modems occurs. The modem cards 70 are connected to the tributary unit (TU) 74 which terminates the connection to the host public switched telephone network 18 (e.g., via one of the lines 47) and handles the signaling of telephony information to, for example, up to 15 subscriber terminals (each via a respective one of 15 of the 16 modems).

The wireless telecommunications between a central terminal 10 and the subscriber terminals 20 could operate on various frequencies. Figure 4 illustrates one possible example of the frequencies which could be used. In the present example, the wireless telecommunication system is intended to operate in the 1.5-2.5GHz Band. In particular the present example is intended to operate in the Band defined by ITU-R (CCIR) Recommendation F.701 (2025-2110MHz, 2200-2290MHz). Figure 4 illustrates the frequencies used

for the uplink from the subscriber terminals 20 to the central terminal 10 and for the downlink from the central terminal 10 to the subscriber terminals 20. It will be noted that 12 uplink and 12 downlink radio channels of 3.5MHz each are provided centred about 2155MHz. The spacing between the receive and transmit channels exceeds the required minimum spacing of 70MHz.

In the present example, as mentioned above, each modem shelf will support 1 frequency channel (i.e. one uplink frequency plus the corresponding downlink frequency). Up to 15 subscriber links may be supported on one frequency channel, as will be explained later. Thus, in the present embodiment, each central terminal 10 can support 60 links, or 120 lines.

Typically, the radio traffic from a particular central terminal 10 will extend into the area covered by a neighboring central terminal 10. To avoid, or at least to reduce interference problems caused by adjoining areas, only a limited number of the available frequencies will be used by any given central terminal 10.

Figure 5A illustrates one cellular type arrangement of the frequencies to mitigate interference problems between adjacent central terminals 10. In the arrangement illustrated in Figure 5A, the hatch lines for the cells 76 illustrate a frequency set (FS) for the cells. By selecting three frequency sets (e.g., where: FS1 = F1, F4, F7, F10; FS2 = F2, F5, F8, F11; FS3 = F3, F6, F9, F12), and arranging that immediately adjacent cells do not use the same frequency set (see, for example, the arrangement shown in Figure 5A), it is possible to provide an array of fixed assignment omnidirectional cells where interference between nearby cells can be avoided. The transmitter power of each central terminal 10 is set such that transmissions do not extend as far as the nearest cell which is using the

same frequency set. Thus each central terminal 10 can use the four frequency pairs (for the uplink and downlink, respectively) within its cell, each modem shelf in the central terminal 10 being associated with a respective RF channel (channel frequency pair).

With each modem shelf supporting one channel frequency (with 15 subscriber links per channel frequency) and four modem shelves, each central terminal 10 will support 60 subscriber links (i.e., 120 lines). The 10 cell arrangement in Figure 5A can therefore support up to 600 ISDN links or 1200 analogue lines, for example. Figure 5B illustrates a cellular type arrangement employing sectored cells to mitigate problems between adjacent central terminals 10. As with Figure 5A, the different type of hatch lines in Figure 5B illustrate different frequency sets. As in Figure 5A, Figure 5B represents three frequency sets (e.g., where: FS1 = F1, F4, F7, F10; FS2 = F2, F5, F8, F11; FS3 = F3, F6, F9, F12). However, in Figure 5B the cells are sectored by using a sectored central terminal (SCT) 13 which includes three central terminals 10, one for each sector S1, S2 and S3, with the transmissions for each of the three central terminals 10 being directed to the appropriate sector among S1, S2 and S3. This enables the number of subscribers per cell to be increased three fold, while still providing permanent fixed access for each subscriber terminal 20.

A seven cell repeat pattern is used such that for a cell operating on a given frequency, all six adjacent cells operating on the same frequency are allowed unique PN codes. This prevents adjacent cells from inadvertently decoding data.

As mentioned above, each channel frequency can support 15 subscriber links. In this example, this is achieved using by multiplexing signals using a Code Division

Multiplexed Access (CDMA) technique. Figure 6 gives a schematic overview of CDMA encoding and decoding.

In order to encode a CDMA signal, base band signals, for example the user signals for each respective subscriber link, are encoded at 80-80N into a 160ksymbols/sec baseband signal where each symbol represents 2 data bits (see, for example the signal represented at 81). This signal is then spread by a factor of 16 using a respective Walsh pseudo random noise (PN) code spreading function 82-82N to generate signals at an effective chip rate of 2.56Msymbols/sec in 3.5MHz. The signals for respective subscriber links are then combined and converted to radio frequency (RF) to give multiple user channel signals (e.g., 85) for transmission from the transmitting antenna 86.

During transmission, a transmitted signal will be subjected to interference sources 88, including external interference 89 and interference from other channels 90. Accordingly, by the time the CDMA signal is received at the receiving antenna 91, the multiple user channel signals may be distorted as is represented at 93.

In order to decode the signals for a given subscriber link from the received multiple user channel, a Walsh correlator 94-94N uses the same pseudo random noise (PN) code that was used for the encoding for each subscriber link to extract a signal (e.g, as represented at 95) for the respective received baseband signal 96-96N. It will be noted that the received signal will include some residual noise. However, unwanted noise can be removed using a low pass filter and signal processing.

The key to CDMA is the application of orthogonal codes that allow the multiple user signals to be transmitted and received on the same frequency at the same time. Once the bit stream is orthogonally isolated using the Walsh codes,

the signals for respective subscriber links do not interfere with each other.

Walsh codes are a mathematical set of sequences that have the function of "orthonormality". In other words, if any Walsh code is multiplied by any other Walsh code, the results are zero.

Figure 7 is a schematic diagram illustrating signal transmission processing stages as configured in a subscriber terminal 20 in the telecommunications system of Figure 1. The central terminal is also configured to perform equivalent signal transmission processing. In Figure 7, an analogue signal from one of a pair of telephones is passed via a two-wire interface 102 to a hybrid audio processing circuit 104 and then via a codec 106 to produce a digital signal into which an overhead channel including control information is inserted at 108. The resulting signal is processed by a convolutional encoder 110 before being passed to a spreader 116 to which the Rademacher-Walsh and PN codes are applied by a RW code generator 112 and PN Code generator 114, respectively. The resulting signals are passed via a digital to analogue converter 118. The digital to analogue converter 118 shapes the digital samples into an analogue waveform and provides a stage of baseband power control. The signals are then passed to a low pass filter 120 to be modulated in a modulator 122. The modulated signal from the modulator 122 is mixed with a signal generated by a voltage controlled oscillator 126 which is responsive to a synthesizer 160. The output of the mixer 128 is then amplified in a low noise amplifier 130 before being passed via a band pass filter 132. The output of the band pass filter 132 is further amplified in a further low noise amplifier 134, before being passed to power control circuitry 136. The output of the power control circuitry

is further amplified in a further low noise amplifier 138 before being passed via a further band pass filter 140 and transmitted from the transmission antenna 142.

Figure 8 is a schematic diagram illustrating the equivalent signal reception processing stages as configured in a subscriber terminal 20 in the telecommunications system of Figure 1. The central terminal is also configured to perform equivalent signal reception processing. In Figure 8, signals received at a receiving antenna 150 are passed via a band pass filter 152 before being amplified in a low noise amplifier 154. The output of the amplifier 154 is then passed via a further band pass filter 156 before being further amplified by a further low noise amplifier 158. The output of the amplifier 158 is then passed to a mixer 164 where it is mixed with a signal generated by a voltage controlled oscillator 162 which is responsive to a synthesizer 160. The output of the mixer 164 is then passed via the de-modulator 166 and a low pass filter 168 before being passed to an analogue to digital converter 170. The digital output of the A/D converter 170 is then passed to a correlator 178, to which the same Rademacher-Walsh and PN codes used during transmission are applied by a RW code generator 172 (corresponding to the RW code generator 112) and a PN code generator 174 (corresponding to PN code generator 114), respectively. The output of the correlator is applied to a Viterbi decoder 180. The output of the Viterbi decoder 180 is then passed to an overhead extractor 182 for extracting the overhead channel information. The output of the overhead extractor 182 is then passed via a codec 184 and a hybrid circuit 188 to a two wire interface 190 where the resulting analogue signals are passed to a selected telephone 192.

At the subscriber terminal 20, a stage of automatic gain control is incorporated at the IF stage. The control

signal is derived from the digital portion of the CDMA receiver using the output of a signal quality estimator to be described later.

Figure 9 is a block diagram of downlink and uplink communication paths between central terminal 10 and subscriber terminal 20. A downlink communication path is established from transmitter 200 in central terminal 10 to receiver 202 in subscriber terminal 20. An uplink communication path is established from transmitter 204 in subscriber terminal 20 to receiver 206 in central terminal 10. Once the downlink and the uplink communication paths have been established in wireless telecommunication system 1, telephone communication may occur between a first user 208 or a second user 210 of subscriber terminal 20 and a user serviced through central terminal 10 over a downlink signal 212 and an uplink signal 214. Downlink signal 212 is transmitted by transmitter 200 of central terminal 10 and received by receiver 202 of subscriber terminal 20. Uplink signal 214 is transmitted by transmitter 204 of subscriber terminal 20 and received by receiver 206 of central terminal 10. Downlink signal 212 and uplink signal 214 are transmitted as CDMA spread spectrum signals.

Receiver 206 and transmitter 200 within central terminal 10 are synchronized to each other with respect to time and phase, and aligned as to information boundaries. In order to establish the downlink communication path, receiver 202 in subscriber terminal 20 should be synchronized to transmitter 200 in central terminal 10. Synchronization occurs by performing an acquisition mode function and a tracking mode function on downlink signal 212. Initially, transmitter 200 of central terminal 10 transmits downlink signal 212. Figure 10 shows the contents of downlink signal 212. Downlink signal 212 includes a code sequence signal 216 for central terminal 10

combined with a frame information signal 218. Code sequence signal 216 is derived from a combination of a pseudo-random noise code signal 220 and a Rademacher-Walsh code signal 222. Although Figure 10 relates specifically to the makeup of the downlink signal, the uplink has the same makeup.

Each receiver 202 of every subscriber terminal 20 serviced by a single central terminal 10 operate off of the same pseudo-random noise code signal as central terminal 10. Each modem shelf 46 in central terminal 10 supports one radio frequency channel and fifteen subscriber terminals 20, each subscriber terminal having a first user 208 and a second user 210. Each modem shelf 46 selects one of sixteen Rademacher-Walsh code signals 222, each Rademacher-Walsh code signal 222 corresponding to a unique subscriber terminal 20. Thus, a specific subscriber terminal 20 will have an identical code sequence signal 218 as downlink signal 212 transmitted by central terminal 10 and destined for the specific subscriber terminal 20.

Downlink signal 212 is received at receiver 202 of subscriber terminal 20. Receiver 202 compares its phase and code sequence to a phase and code sequence within code sequence signal 216 of downlink signal 212. Central terminal 10 is considered to have a master code sequence and subscriber terminal 20 is considered to have a slave code sequence. Receiver 202 incrementally adjusts the phase of its slave code sequence to recognize a match to master code sequence and place receiver 202 of subscriber terminal 20 in phase with transmitter 200 of central terminal 10. The slave code sequence of receiver 202 is not initially synchronized to the master code sequence of transmitter 200 and central terminal 10 due to the path delay between central terminal 10 and subscriber terminal 20. This path delay is caused by the geographical

separation between subscriber terminal 20 and central terminal 10 and other environmental and technical factors affecting wireless transmission.

Figure 11 illustrates how receiver 202 of subscriber terminal 20 adjusts its slave code sequence to match the master code sequence of transmitter 200 in central terminal 10. Receiver 202 increments the phase of the slave code sequence throughout the entire length of the master code sequence within downlink signal 212 and determines a signal quality estimate by performing a power measurement on the combined power of the slave code sequence and the master code sequence for each incremental change in the phase of the slave code sequence. The length of the master code sequence is approximately 100 microseconds based on a chip period of 2.56 MegaHertz. The phase of the slave code sequence is adjusted by one half of a chip period for each incremental interval during the acquisition phase. Receiver 202 completes a first acquisition pass when it identifies a correlation peak where the combined power reaches a maximum value. Receiver 202 performs a second acquisition pass throughout the entire length of the code sequence to verify identification of the maximum value of the combined power at the correlation peak. The approximate path delay between subscriber terminal 20 and central terminal 10 is determined when the correlation peak position is identified in the acquisition mode.

Once acquisition of downlink signal 212 is achieved at receiver 202, fine adjustments are made to the phase of the slave code sequence in order to maintain the phase matching of the slave code sequence with the master code sequence in the tracking mode. Fine adjustments are made through one sixteenth of a chip period incremental changes to the phase of the slave code sequence. Fine adjustments may be performed in either forward (positive) or backward

(negative) directions in response to the combined power measurements made by receiver 202. Receiver 202 continuously monitors the master code sequence to ensure that subscriber terminal 20 is synchronized to central terminal 10 for the downlink communication path.

Figure 12 shows a graph of the combined power curve measured by receiver 202 during the acquisition mode and the tracking mode. The maximum value of the combined power occurs at the correlation peak 219 of the combined power curve. It should be noted that the peak 219 may not be as well defined as in Figure 12, but may be flattened at the top, more in the form of a plateau. This is the point where the slave code sequence of receiver 202 is in phase with and matches the master code sequence of transmitter 200. Measurements resulting in combined power values that occur off of correlation peak 219 require incremental adjustments to be made to the slave code sequence. A fine adjustment window is established between an early correlator point 221 and a late correlator point 223. An average power measurement is performed at early correlator point 221 and at late correlator point 223. Since early correlator point 221 and late correlator point 223 are spaced one chip period apart, an error signal is produced upon calculating the difference between the average powers of early correlator point 221 and late correlator point 223 that is used to control the fine adjustments to the phase of the slave code sequence.

After acquiring and initiating tracking on the central terminal 10 master code sequence of code sequence signal 216 within downlink signal 212, receiver 202 enters a frame alignment mode in order to establish the downlink communication path. Receiver 202 analyzes frame information within frame information signal 218 of downlink signal 212 to identify a beginning of frame position for

downlink signal 212. Since receiver 202 does not know at what point in the data stream of downlink signal 212 it has received information, receiver 202 must search for the beginning of frame position in order to be able to process information received from transmitter 200 of central terminal 10. Once receiver 202 has identified one further beginning of frame position, the downlink communication path has been established from transmitter 200 of central terminal 10 to receiver 202 of subscriber terminal 20.

Figure 13 shows the general contents of frame information signal 218. Frame information signal 218 includes an overhead channel 224, a first user channel 226, a second user channel 228, and a signalling channel 230 for each frame of information transported over downlink signal 212. Overhead channel 224 carries control information used to establish and maintain the downlink and uplink communication paths. First user channel 226 is used to transfer traffic information to first user 208. Second user channel 228 is used to transfer traffic information to second user 210. Signalling channel 230 provides the signalling information to supervise operation of subscriber terminal 20 telephony functions. Overhead channel 224 occupies 16 kilobits per second of a frame of information, first user channel 226 occupies 64 kilobits per second of a frame of information, second user channel 228 occupies 64 kilobits per second of a frame of information, and signalling channel 230 occupies 16 kilobits per second of a frame of information.

Figure 14 shows how overhead channel 224 is inserted into the data stream of downlink signal 212. The data stream of downlink signal 212 is partitioned into twenty bit subframes. Each twenty bit subframe has two ten bit sections. A first ten bit section includes an overhead bit, a signalling bit, and eight first user bits. A second

ten bit section includes an overhead bit, a signalling bit, and eight second user bits. This twenty bit subframe format is repeated throughout an entire four millisecond frame of information. Thus, an overhead bit occupies every tenth bit position of frame information in the data stream of downlink signal 212.

Overhead channel 224 includes eight byte fields - a frame alignment word 232, a code synchronization signal 234, a power control signal 236, an operations and maintenance channel signal 238, and four reserved byte fields 242. Frame alignment word 232 identifies the beginning of frame position for its corresponding frame of information. Code synchronization signal 234 provides information to control synchronization of transmitter 204 in subscriber terminal 20 to receiver 206 in central terminal 10. Power control signal 236 provides information to control transmitting power of transmitter 204 in subscriber terminal 20. Operations and maintenance channel signal 238 provides status information with respect to the downlink and uplink communication paths and a path from the central terminal to the subscriber terminal on which the communication protocol which operates on the modem shelf between the shelf controller and the modem cards also extends.

In order to identify two successive beginning of frame positions, receiver 202 of subscriber terminal 20 searches through the ten possible bit positions in the data stream of downlink signal 212 for overhead channel 224 and frame alignment word 232. Receiver 202 initially extracts a first bit position of every ten bit section of frame information to determine if overhead channel 224 has been captured. If frame alignment word 232 has not been identified after a predetermined period of time from the extraction of the first bit position, receiver 202 will

repeat this procedure for the second bit position of each ten bit section and subsequent bit positions until frame alignment word 232 has been identified. An example of a frame alignment word 232 which receiver 202 would search for is binary 00010111. Once the correct bit position yields frame alignment word 232, receiver 202 attempts to identify two successive beginning of frame positions. A downlink communication path is established upon the successful identification of two successive beginning of frame positions in response to recognition of successive frame alignment words 232 in the data stream of downlink signal 212.

Receiver 202 continues to monitor the appropriate bit position in order to recognize subsequent frame alignment words 232 for subsequent frames of information. If receiver 202 fails to recognize a frame alignment word 232 for three successive frames, then receiver 202 will return to the search process and cycle through each of the bit positions of the ten bit section until identifying two successive beginning of frame positions through recognition of two successive frame alignment words 232 and reestablishing frame alignment. Failure to recognize three successive frame alignment words 232 may result from a change in the path delay between central terminal 10 and subscriber terminal 20. Receiver 202 will also return to the search process upon an interruption in the downlink communication path from transmitter 200 in central terminal 10 to receiver 202 in subscriber terminal 20.

Upon establishing the downlink communication path from central terminal 10 to subscriber terminal 20 through proper code sequence phase synchronization and frame alignment, wireless telecommunication system 1 performs procedures to establish the uplink communication path from transmitter 204 in subscriber terminal 20 to receiver 206

in central terminal 10. Initially, transmitter 204 is powered off until the downlink communication path has been established to prevent transmitter interference of central terminal communications with other subscriber terminals. After the downlink communication path is established, transmitting power of transmitter 204 is set to a minimum value on command from the central terminal CT via power control channel 236 of overhead channel 224. Power control signal 236 controls the amount of transmitting power produced by transmitter 204 such that central terminal 10 receives approximately the same level of transmitting power from each subscriber terminal 20 serviced by central terminal 10.

Power control signal 236 is transmitted by transmitter 200 of central terminal 10 in overhead channel 224 of frame information signal 218 over downlink signal 212. Receiver 202 of subscriber terminal 20 receives downlink signal 212 and extracts power control signal 236 therefrom. Power control signal 236 is provided to transmitter 204 of subscriber terminal 20 and incrementally adjusts the transmitting power of transmitter 204. Central terminal 10 continues to incrementally adjust the transmitting power of transmitter 204 until the transmitting power falls within a desired threshold range as determined by receiver 206. Adjustments to the transmitting power initially occur in a coarse adjustment mode having one decibel increments until the transmitting power falls within the desired threshold range. Upon turning transmitter 204 on, the transmitting power is gradually ramped up in intensity through incremental adjustments in order to avoid interference of central terminal communications with other subscriber terminals.

Figure 15 shows an example decoding scheme for power control signal 236. After the transmitting power of

transmitter 204 in subscriber terminal 20 reaches the desired threshold range, receiver 206 in central terminal 10 continues to monitor the amount of transmitting power from transmitter 204 for any changes resulting from power fluctuations, and variations in the path delay between central terminal 10 and subscriber terminal 20, et al. If the transmitting power falls below or exceeds the desired threshold range, central terminal 10 will send an appropriate power control signal 236 to increase or decrease the transmitting power of transmitter 204 as needed. At this point, adjustments made to return the transmitting power to the desired threshold range may occur in a fine adjustment mode having 0.1 decibel increments. Upon an interruption in the downlink or uplink communication paths, central terminal 10 may command transmitter 204 to return to a previous transmitting power level through recovery of parameters stored in a memory in subscriber terminal 20 in order to facilitate reestablishment of the appropriate communication path.

To fully establish the uplink communication path from subscriber terminal 20 to central terminal 10, transmitter 204 in subscriber terminal 20 should be synchronized to receiver 206 in central terminal 10. Central terminal 10 controls the synchronization of transmitter 204 through code synchronization signal 234 in overhead channel 224 of frame information signal 218. Code synchronization signal 234 incrementally adjusts a phase of the slave code sequence of transmitter 204 to match the phase of the master code sequence of receiver 206. Synchronization of transmitter 204 is performed in a substantially similar manner as synchronization of receiver 202.

Code synchronization signal 234 is transmitted by transmitter 200 in central terminal 10 in overhead channel 224 of frame information signal 218 over downlink signal

212. Receiver 202 of subscriber terminal 20 receives downlink signal 212 and extracts code synchronization signal 234 therefrom. Code synchronization signal 234 is provided to transmitter 204 for incrementally adjustment of the phase of the slave code sequence of transmitter 204. Central terminal 10 continues to incrementally adjust the phase of the slave code sequence of transmitter 204 until receiver 206 recognizes a code and phase match between the slave code sequence of transmitter 204 and the master code sequence of central terminal 10.

Receiver 206 performs the same power measurement technique in determining a phase and code match for transmitter 204 synchronization as performed for receiver 202 synchronization. Adjustments to the phase of the slave code sequence of transmitter 204 initially occur in a coarse adjustment mode having one half of a chip rate increments until receiver 206 identifies the maximum power position of the combined power of the master code sequence and the slave code sequence of transmitter 204.

Figure 16 shows an example decoding scheme for code synchronization signal 234. After identification and verification of a phase and code match of the slave code sequence to the master code sequence, receiver 206 continues to monitor uplink signal 214 for changes in the phase of the slave code sequence of transmitter 204 resulting from variations in the path delay between central terminal 10 and subscriber terminal 20. If further adjustments are needed to the phase of the slave code sequence of transmitter 204, central terminal 10 will send appropriate code synchronization signals 234 to increase or decrease the phase of the slave code sequence of transmitter 204 as needed. At this point, adjustments made to the phase of the slave code sequence of transmitter 204 may occur in a fine adjustment mode having one sixteenth of

a chip rate increments. Upon an interruption in the downlink or uplink communication paths, central terminal 10 may command transmitter 204 to return to a previous slave code sequence phase value through recovery of parameters stored in a memory in subscriber terminal 20 in order to facilitate reestablishment of the appropriate communication path.

After synchronization of transmitter 204 is achieved, receiver 206 performs frame alignment on uplink signal 214 in a similar manner as frame alignment is performed by receiver 202 during establishment of the downlink communication path. Once receiver 206 recognizes two successive frame alignment words and obtains frame alignment, the uplink communication path has been established. Upon establishing both the downlink and the uplink communication paths, information transfer between first user 208 or second user 210 of subscriber terminal 20 and users coupled to central terminal 10 may commence.

Wireless telecommunication system 1 is capable of adjusting the transmitting power level and the transmit rate to one of two settings for each of three different system operating modes. The system operating modes are acquisition, standby and traffic. Adjustments in the transmitting power and the transmit rate make it possible to reduce and minimize interference with other subscriber terminals. Improvements in link establishment time are also achieved. The transmitting power level is decoded in power control signal 236 and the transmit rate is decoded in code synchronization signal 234.

The transmitting power for both downlink signal 212 and uplink signal 214 can be set to either a nominal 0 decibel high power level or a reduced -12 decibel low power level. The transmit rate for both downlink signal 212 and uplink signal 214 can be set to a low rate of 10 kilobits

per second or a high rate of 160 kilobits per second. When switched to the high rate of 160 kilobits per second, user traffic and overhead information are spread such that one information symbol results in the transmission of 16 chips. Correlation is performed over 16 chips, yielding a processing gain of 12 decibels. When switched to the low rate of 10 kilobits per second, only overhead information is spread such that one overhead symbol results in the transmission of 256 chips. Correlation is performed over 256 chips, yielding a processing gain of 24 decibels.

Figure 17 show the transmitting power and transmit rate for each of the three system operating modes. At power up or whenever the downlink or uplink communication paths are lost, wireless telecommunication system 1 enters the acquisition mode. During the acquisition mode, the transmitting power of the downlink and uplink transmitters are maximized as well as the correlator processing gain. This maximizes the signal to noise ratio at the correlator output, increasing the amplitude of the correlation peak 219 for easier identification and minimal risk of false acquisition. Since only overhead information is needed in the acquisition mode, the transmit rate is at the low rate level of 10 kilobits per second.

When the downlink and the uplink communication paths are acquired, wireless telecommunication system 1 enters the standby mode. In the standby mode, the transmitting power of the downlink and uplink transmitters are reduced by 12 decibels. This reduction in transmitting power minimizes the interference to other subscriber terminals while still maintaining synchronization. The transmit rate remains at the low rate level to allow exchange of control information between central terminal 10 and subscriber terminal 20 over overhead channel 224.

When either an incoming or outgoing call is detected, a message is sent from the originating terminal to the destination terminal indicating that the downlink and uplink communication paths are required for the transmission of user traffic information. At this point, wireless telecommunication system 1 enters into the traffic mode. During the traffic mode, the transmitting power of both the downlink and uplink communication paths is increased to the high power level and the transmit rate is increased to the high rate level of 160 kilobits per second to facilitate information transfer between originating and destination terminals. Upon detection of call termination, a message is sent from the terminating terminal to the other terminal indicating that the downlink and uplink communication paths are no longer required. At this point, wireless telecommunication system 1 reenters the standby mode. Code synchronization and frame alignment tracking is performed in both the standby mode and the traffic mode.

Figure 18 is a detailed block diagram of receiver 202 and transmitter 204 in subscriber terminal 20. Receiver 202 receives downlink signal 212 at an RF receive interface 250. RF receive interface 250 separates the spread spectrum signal into I and Q signal components. RF receive interface 250 band pass filters each of the I and Q signal components by removing portions above approximately half of receiver 202 bandwidth of 3.5 MegaHertz. RF receive interface 250 low pass filters the I and Q signal components to reject image frequencies and prevent signal aliasing. The I and Q signal components are placed into digital format by an analog to digital converter 252. The sampling frequency of analog to digital converter 252 is four times the chip period, or 10.24 MegaHertz, with an eight bit resolution.

The digital I and Q signal components are stepped to a rate of 5.12 MegaHertz by a down converter 254. A code generator and despreader 256 performs the synchronization acquisition and tracking functions previously described to synchronize the phase of the Rademacher-Walsh and pseudo-random noise code sequence of receiver 202 to that of downlink signal 212. A digital signal processor 258 controls the phase of the slave code sequence through a code tracker 260 and a carrier tracker 262. An automatic gain control unit 264 produces an automatic gain control signal to control the gain of RF receive interface 250. Code generator and despreader 256 generates the I and Q 160 kilobits per second of frame information for further synchronization by a node sync interface 266 under the control of a node sync logic unit 268. Node sync interface 266, through node sync logic unit 268, determines whether the I and Q channels should be swapped, as they may be received in four different ways.

Viterbi decoder 270 provides forward error correction on the I and Q channels and generates an error corrected 160 kilobits per second data signal after a 71 symbol delay. The error corrected signal is processed by a frame aligner and extractor 272 determines frame alignment and extracts power control signal 236, code synchronization 234, and operations and maintenance channel signal 238. Frame aligner and extractor 272 also extracts first user channel 226 and second user channel 228 for traffic transmission towards first user 208 an second user 210, and signaling channel 230 for processing by high level data link controller 274 and a microcontroller 276. Frame aligner and extractor 272 also provides alarm and error indications upon detecting a loss in frame alignment. A non-volatile random access memory 278 stores system parameter information for subsequent insertion through an

arbitrator 280 in the event of link loss in order to facilitate link reestablishment. Arbitrator 280 also provides an interface between digital signal processor 258 and microcontroller 276.

In the transmit direction, a frame inserter 282 receives first user traffic and second user traffic from first user 208 and second user 210, signaling channel 230 information from high level data link controller 274, and operations and maintenance channel 238 information from microcontroller 276. Frame inserter generates frame information signal 218 for uplink signal 214 for processing by a convolutional encoder 284. Convolutional encoder 284 doubles the data rate of frame information signal 218 to provide forward error correction. A spreader 286 splits the 320 kilobits per second signal of convolutional encoder 284 into two 160 kilobits per second I and Q signals and exclusively ORs these signals with the spreading sequence generated by a code generator 288 in response to a system clock generated by clock generator 290 as adjusted by code synchronization signal 234. Code generator 288 generates one of sixteen Rademacher-Walsh functions exclusive ORed with a pseudo-random sequence having a pattern length of 256 with a chip rate of 2.56 MegaHertz. The pseudo-random sequence should match that of central terminal 10, but is adjustable under software control to provide reliable rejection of signals from other bands or other cells.

Spreader 286 supplies the I and Q signals to an analog transmitter 290. Analog transmitter 290 produces pulsed I and Q signals for an RF transmit interface 292. Transmit power is generated by first establishing a control voltage from a digital to analog converter in response to power control signal 236 extracted from overhead channel 224. This control voltage is applied to the power control inputs of analog transmitter 290 and RF transmit interface 292.

Power control of 35 decibels is obtainable in both analog transmitter 290 and RF transmit interface 292. RF transmit interface 292 includes a step attenuator that provides 2 decibel steps of attenuation over a 30 decibel range. This attenuator is used to switch between high and low power levels. On power up, maximum attenuation is selected to minimize the transmitting power of transmitter 204.

Figure 19 is a block diagram of a CDMA signal processing circuit 100 within spreader 286. CDMA signal processing circuit 300 includes a summer circuit 302 that receives a plurality of CDMA signals from a plurality of channels 304. Summer circuit 302 generates a summed signal 306 that is applied to a clipping circuit 308. Clipping circuit 308 generates a clipped signal 310 that is applied to an I digital to analog processing circuit 312 and a Q digital to analog processing circuit 314. Digital to analog processing circuit 312 generates an I signal that is filtered by an I filter 316. Digital to analog processing circuit 314 generates a Q signal that is filtered by a Q filter 318.

In operation, CDMA signal processing circuit 300 receives CDMA signals from the plurality of channels 304 at summer circuit 302. Each CDMA signal has a disable value, a power magnitude value, and power direction value. The disable value determines whether a CDMA signal is present on the particular channel. The power magnitude value identifies the relative power of the CDMA signal. The power magnitude value preferably has a low power value of 1 and a high power value of 4. The power direction value determines the positive or negative direction of the relative CDMA signal power and which of the I or Q signals the CDMA signal corresponds. Summer circuit 302 combines the power values of each CDMA signal from the plurality of channels 304 to generate summed signal 306. For a sixteen

channel circuit, summed signal 306 may range from -64 to +64 according to the power magnitude and direction values.

Clipping circuit 308 generates a clipped signal 310 in response to summed signal 306. Clipping circuit 308 removes a portion of summed signal 306 to improve handling of more frequently occurring values within a desired threshold range. Figure 20 shows selected values of summed signal 306 and selected values of clipped signal 310 generated in response thereto. Clipping circuit 308 removes that portion of summed signal 306 above and below a magnitude of +/- 31. A summed signal 306 occurring above the threshold magnitude of +31 is set at the +31 magnitude level. A summed signal occurring below the threshold magnitude of -31 is set at the -31 magnitude level.

Removal of the portion of summed signal 306 outside the desired threshold range also eliminates noise producing sidebands from appearing on clipped signal 310 and increases the signal magnitude according to the desired threshold range. Elimination of noise producing sidebands results in more accurate and reliable I and Q signals. Though shown with a desired threshold range of approximately one half of summed signal 306, clipping circuit 308 may use a different threshold range selected to provide elimination of noise producing sidebands and improved handling of frequently occurring values of summed signal 306.

Digital to analog processing circuits 312 and 314 each receive clipped signal 310 generated by clipping circuit 308. Digital to analog processing circuits 312 and 314 converts clipped signal 310 into a half width encoded format. Figure 21 shows an example of the half width encoded format. At each chip period, clipped signal 310 is converted into a half width return to zero format wherein the first half of the chip period contains the information

and the second half of the chip period contains no information. By using the half width encoded format, increased power is obtained in the permitted band of frequencies for transmitted signals. More energy and information is within the passband of clipped signal 310 and the half width encoded format aids in information decoding at a far end receiver. After conversion to the half width encoded format, digital to analog processing circuits 312 and 314 convert clipped signal 310 into analog I and Q components, respectively.

To generate final I and Q signals, the outputs of digital to analog processing circuits 312 and 314 are processed by I filter 316 and Q filter 318, respectively. Filters 316 and 318 are used to significantly reduce inter-symbol interference between each half width encoded piece of the I and Q analog signals. Figure 22 shows an example of inter-symbol interference. Identifying transitions between half width encoded portions of an analog signal is important in reading and identifying information encoded in the analog signal. Preventing interference in the transition from one symbol of information to another aids in accurately and reliably reading information from analog signals. Filters 316 and 318 provide a smoother rolloff and transition in the analog I and Q signals from one symbol to the next. A ninth order Besel filter operation may be performed to minimize rolloff from a first symbol from affecting the next symbol. The ninth order Besel filter provides a sufficient linear characteristic to achieve a desired reduction in inter-symbol interference.

In summary, a CDMA signal processing circuit combines CDMA signals from multiple channels to generate a summed signal in accordance with a power magnitude value and a power direction value associated with each CDMA signal. A portion of the summed signal outside a desired threshold

range is removed to generate a clipped signal having noise producing sidebands from the outer area of the summed signal eliminated and to improve handling of frequently occurring values of the summed signal. The clipped signal is converted into a half width encoded format by a digital to analog processing circuit to increase desired frequency band power. The digital to analog processing circuit transforms the half width encoded clipped signal into a corresponding I and Q analog signal. The I and Q signals are filtered to reduce inter-symbol interference between symbols of information half width encoded into the I and Q analog signals.

Thus, there has been provided in accordance with the present invention, an apparatus and method of processing CDMA signals that satisfy the advantages set forth above. Although the preferred embodiment has been described in detail, it should be understood that various changes, substitutions, and alterations can be made herein by one of ordinary skill in the art without departing from the scope of the present invention.

WHAT IS CLAIMED IS:

1. A method of processing CDMA signals, comprising the steps of:

performing a spreading function on CDMA signals from a plurality of channels;

combining the CDMA signals of the plurality of channels to create a summed signal;

removing a portion of the summed signal above and below a desired threshold range to create a clipped signal.

2. The method of Claim 1, wherein the CDMA signals have a disable value, a power magnitude value, and a power direction value used in determining the summed signal.

3. The method of Claim 1, wherein the power magnitude value has a first level representing an on-hook condition and a second level value representing an off-hook condition.

4. The method of Claim 1, wherein the portion of the summed signal removed is sufficient to prevent noise producing sidebands from appearing on the clipped output signal.

5. The method of Claim 2, wherein the summed signal ranges in value from -64 to +64 in response to a disabled value of zero, a power magnitude value of 1/4, and a power direction value of positive or negative.

6. The method of Claim 1, wherein said threshold range is approximately one half the total range of the summed signal.

7. The method of Claim 1, further comprising the step of:

converting the summed signal into two separate data channels for modulating a radio frequency carrier transmission signal, each of the two separate data channels carrying information in a half-width pulse configuration, wherein a first half of the pulse contains valid information and a second half of the pulse has a return to zero format.

8. The method of Claim 7, further comprising the step of:

filtering the two separate data channels to remove interference outside of a desired radio frequency bandwidth.

9. The method of Claim 8, wherein the filtering step is performed by a ninth order Bessel low pass filtering operation.

10. The method of Claim 8, wherein the filtering step has properties sufficient to reduce inter-symbol interference between each half width pulse.

11. A method of processing CDMA signals, comprising the steps of:

performing a spreading function on CDMA signals from a plurality of channels;

combining the CDMA signals of the plurality of channels to create a summed signal;

converting the summed signal into two separate data channels for modulating a radio frequency carrier transmission signal, each of the two separate data channels carrying information in a half-width pulse configuration, wherein a first half of the pulse contains valid information and a second half of the pulse has a return to zero format.

12. The method of Claim 11, further comprising the step of:

filtering the two separate data channels to remove interference outside of a desired radio frequency bandwidth.

13. The method of Claim 12, wherein the filtering step is performed by a ninth order Bessel low pass filtering operation.

14. The method of Claim 12, wherein the filtering step has properties sufficient to reduce inter-symbol interference between each half width pulse.

15. The method of Claim 11, comprising the steps of:

removing a portion of the summed signal above and below a desired threshold range to create a clipped signal.

16. The method of Claim 15, wherein the CDMA signals have a disable value, a power magnitude value, and a power direction value used in determining the summed signal.

17. The method of Claim 16, wherein the power magnitude value has a first level representing an on-hook condition and a second level representing an off-hook condition.

18. The method of Claim 15, wherein the portion of the summed signal removed is sufficient to prevent noise producing sidebands from appearing on the clipped output signal.

19. The method of Claim 16, wherein the summed signal ranges in value from -64 to +64 in response to a disabled value of zero, a power magnitude value of 1 and 4, and a power direction value of positive or negative.

20. The method of Claim 15, wherein the desired threshold range is approximately one half the total range of the summed signal.

21. An apparatus for processing CDMA signals, comprising:

a summer circuit operable to combine CDMA signals from a plurality of channels, the summer circuit operable to generate a summed signal therefrom;

a clipping circuit operable to remove a portion of the summed signal above and below a desired threshold range, the clipping circuit operable to generate a clipped signal therefrom;

a digital to analog processing circuit operable to convert the clipped signal into a half width encoded format, the half width encoded format having information contained in a first half of a signal pulse and no information in a second half of the signal pulse, the digital to analog processing circuit operable to convert the clipped signal in the half width encoded format to an analog signal;

a filter operable to reduce inter-symbol interference in the analog signal.

22. The apparatus of Claim 21, wherein the filter performs a ninth order Besel low pass filtering operation to smooth out a rolloff from one symbol to another.

23. The apparatus of Claim 21, wherein the clipping circuit removes the portion of the summed signal sufficient to prevent noise producing sidebands from appearing on the clipped output signal.

24. The apparatus of Claim 23, wherein each CDMA signals has a disable value, a power magnitude value, or a power direction value for use in determining the summed signal, the summed signal ranging in value from -64 to +64 in response to a disabled value of zero, a power magnitude value of 1 and 4, and a power direction value of positive and negative, the desired threshold range being approximately one half the total range of the summed signal.

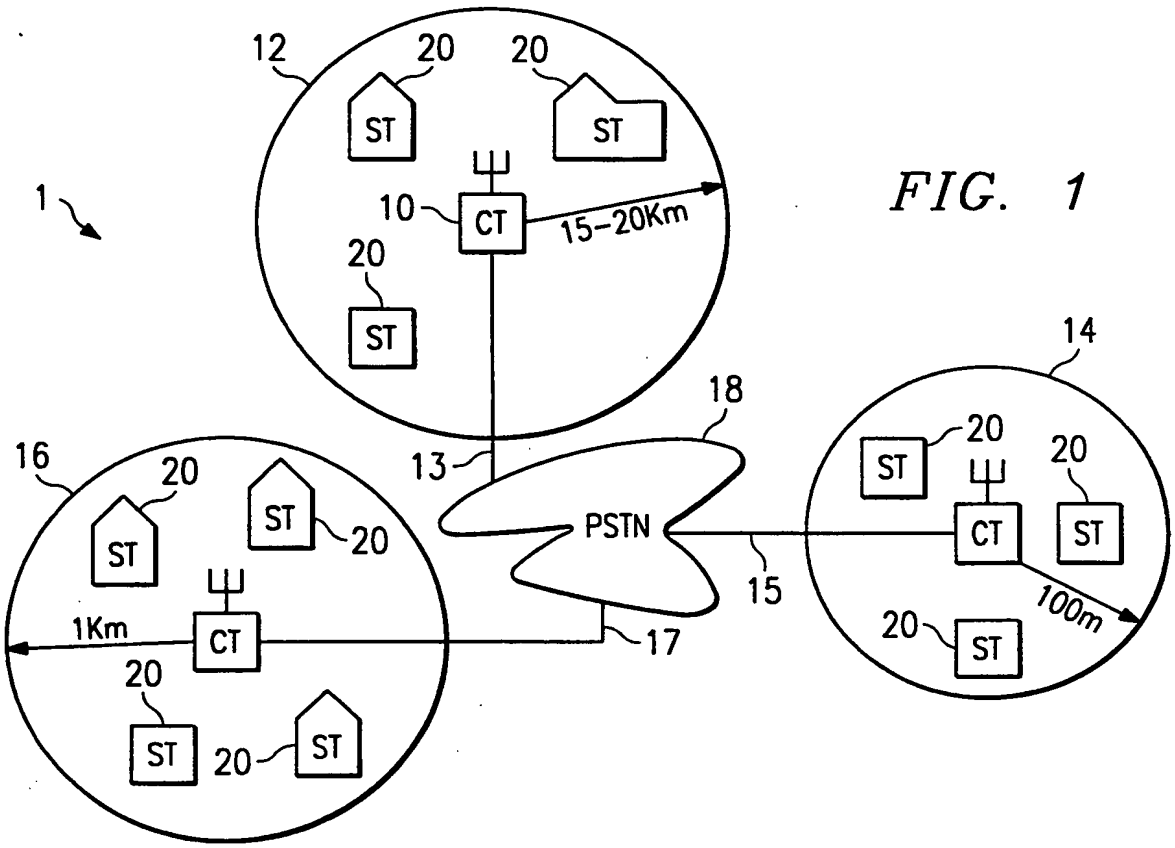


FIG. 1

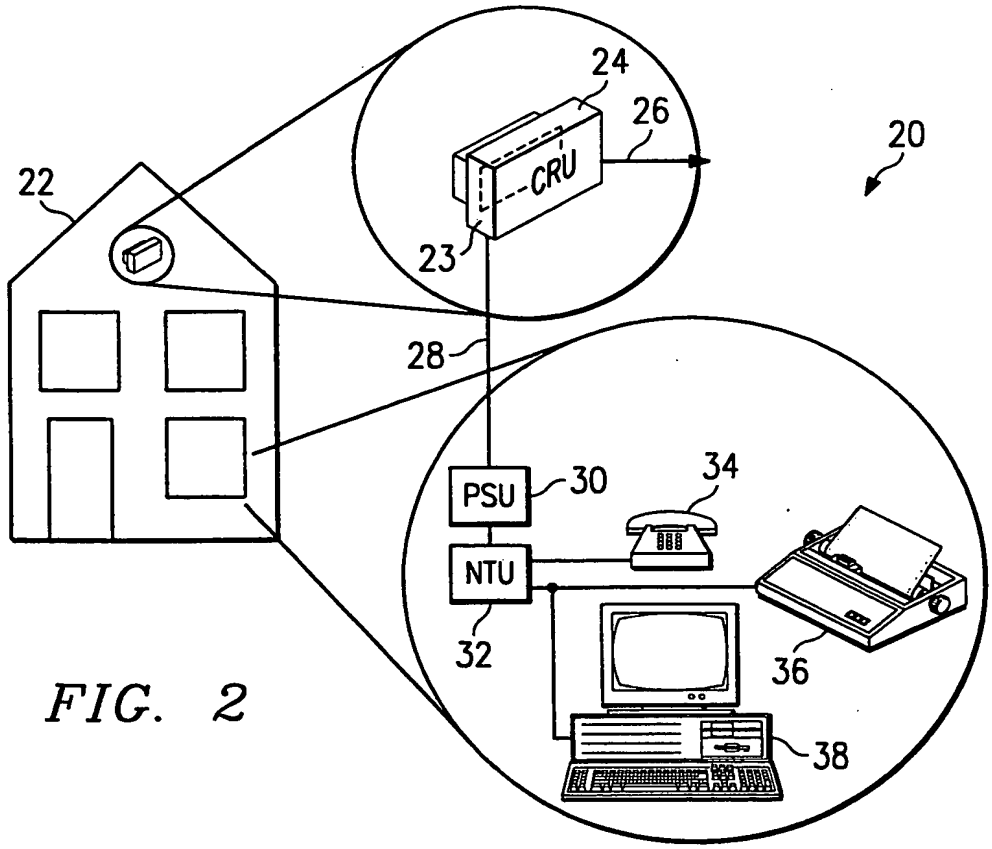


FIG. 2

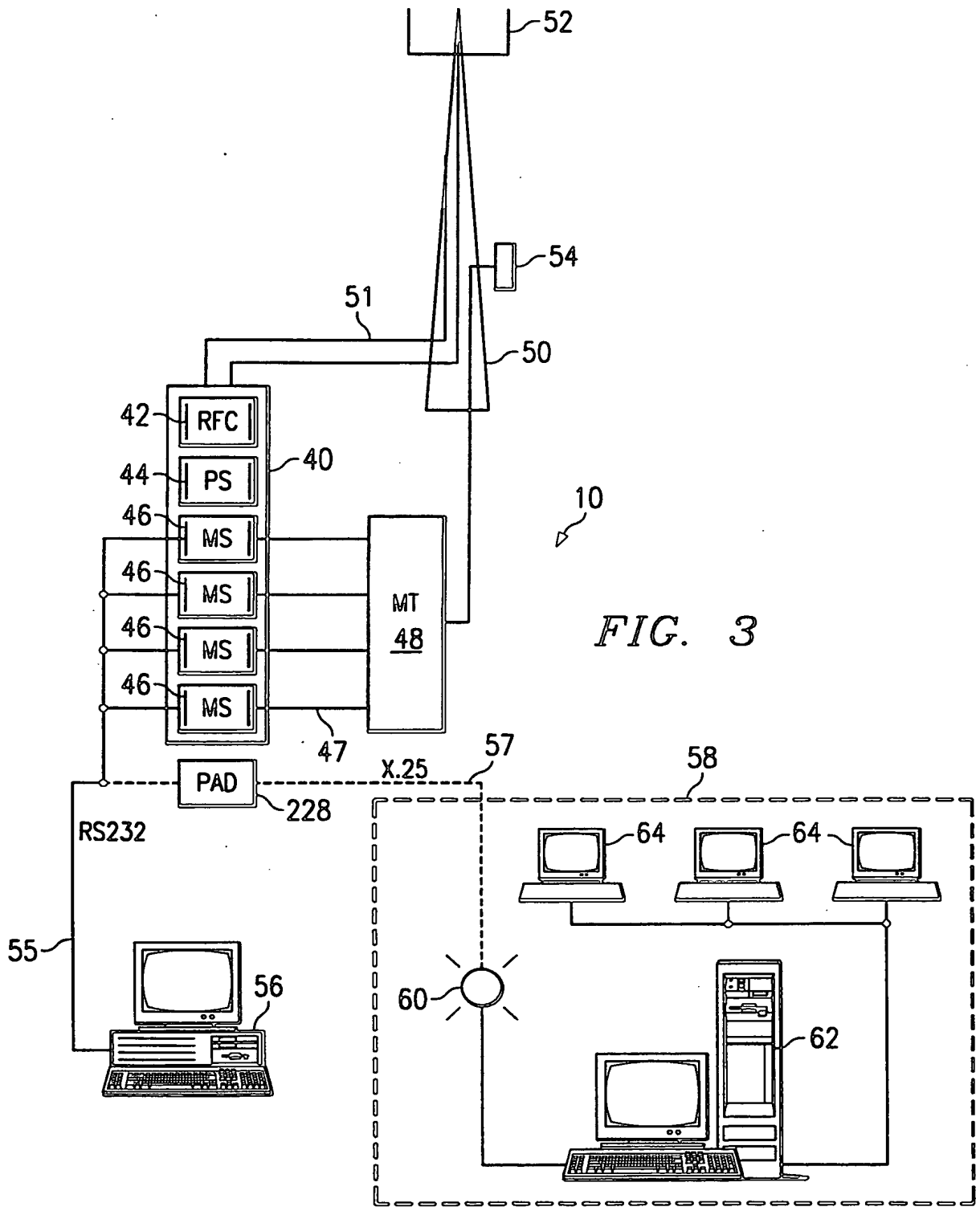


FIG. 3

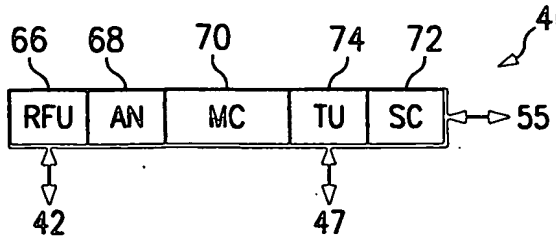


FIG. 3A

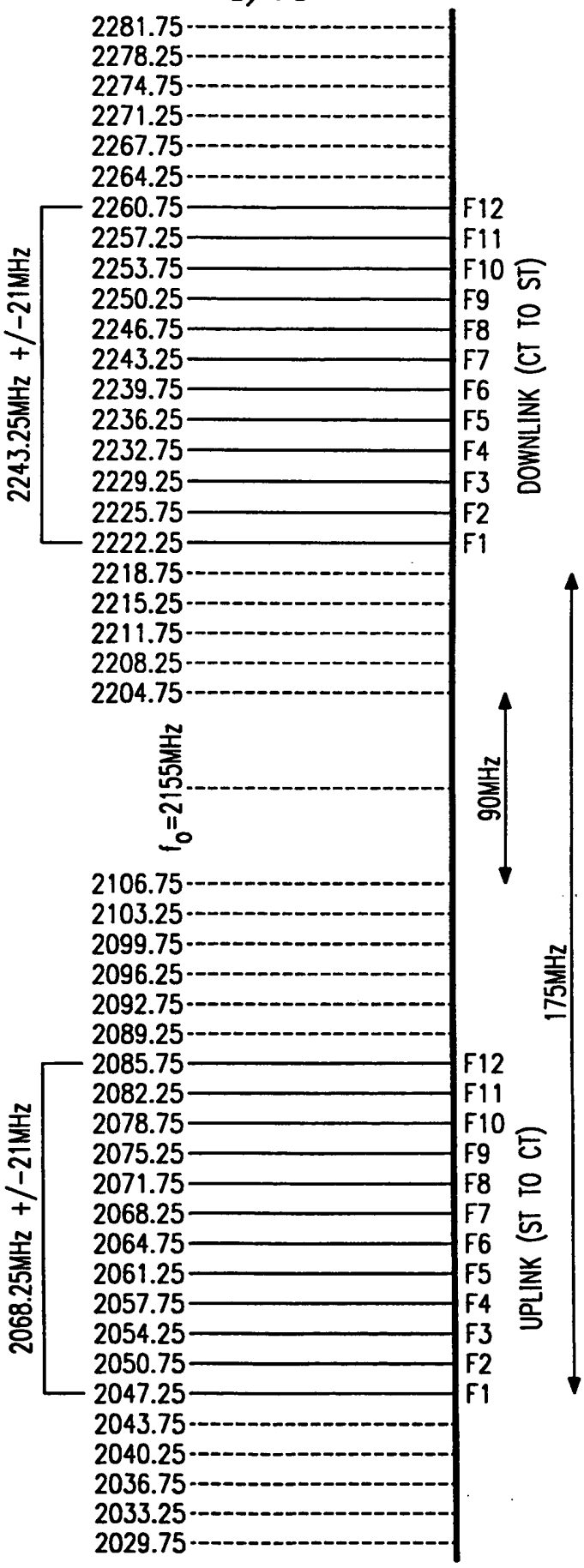
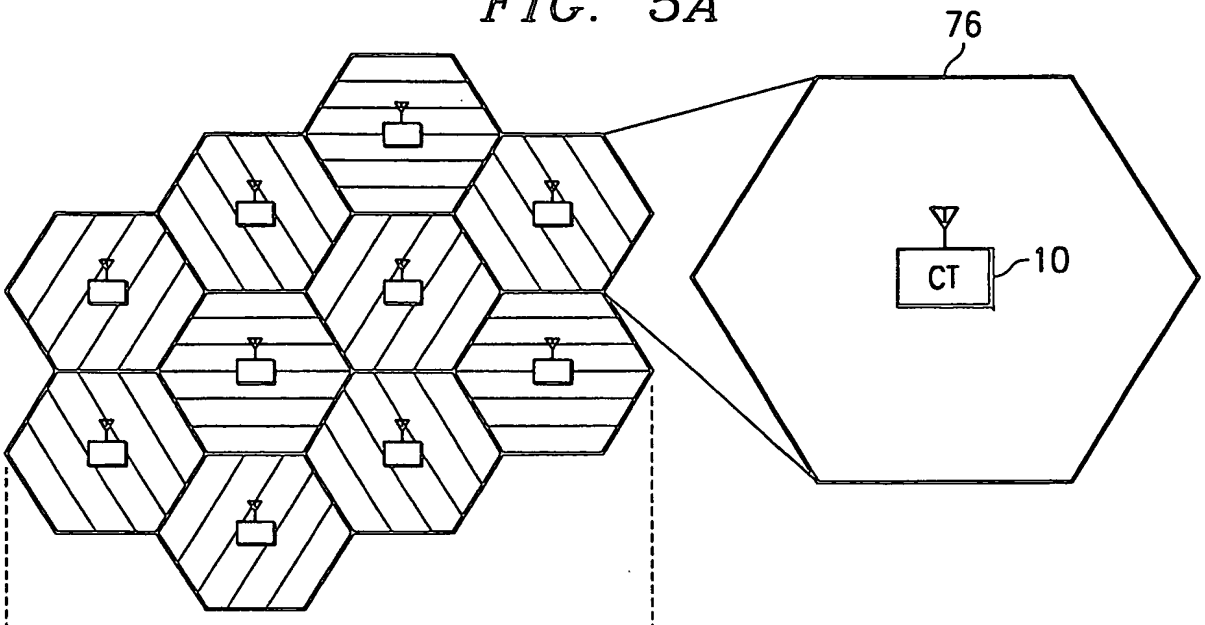


FIG. 4

FIG. 5A



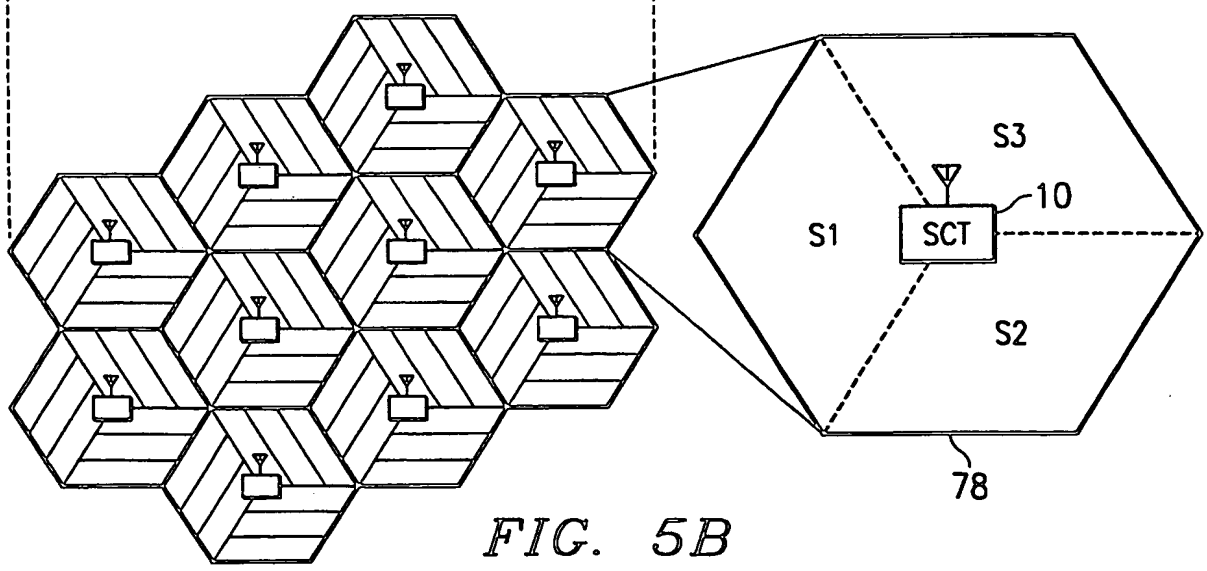


FIG. 5B

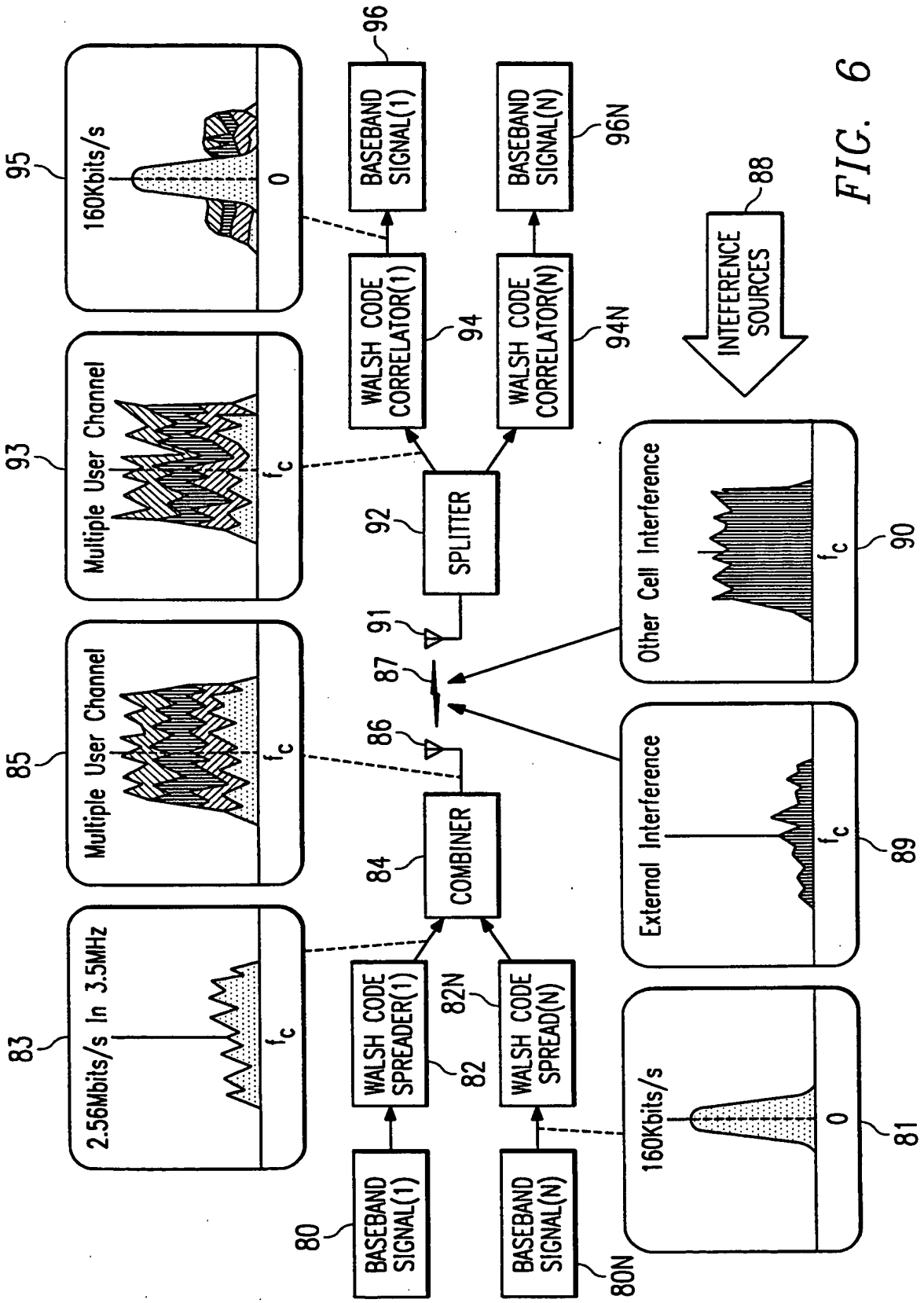


FIG. 6

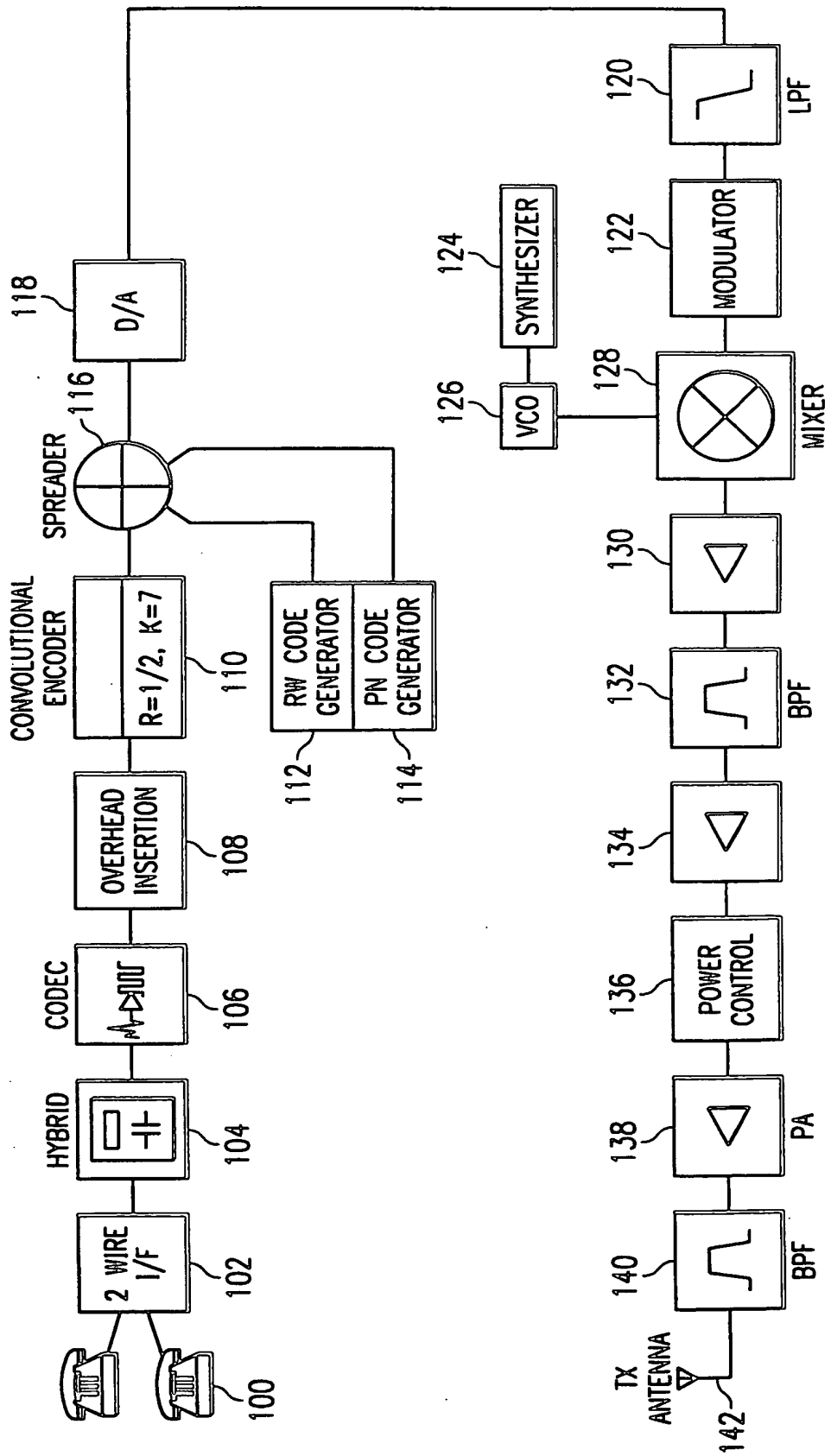


FIG. 7

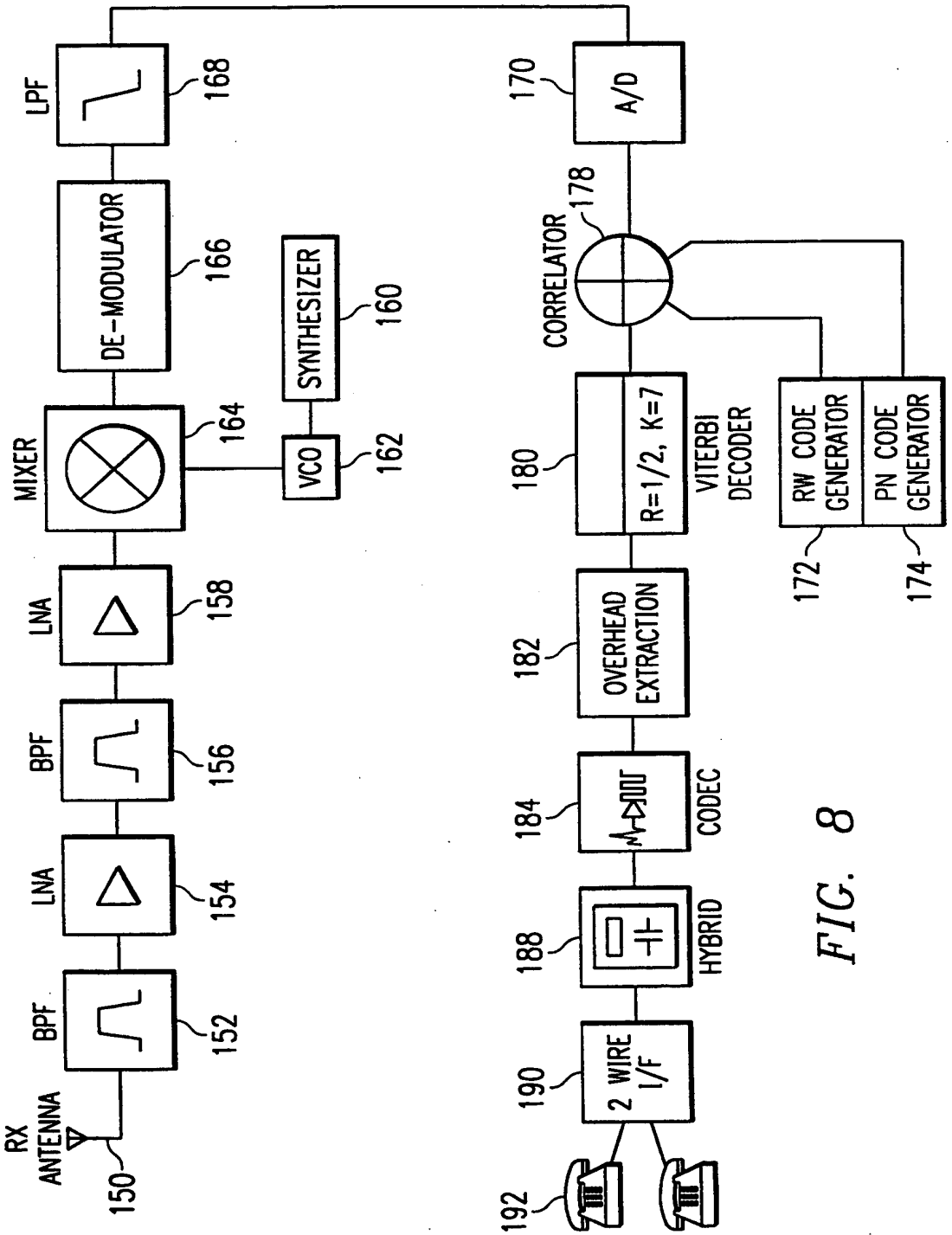


FIG. 8

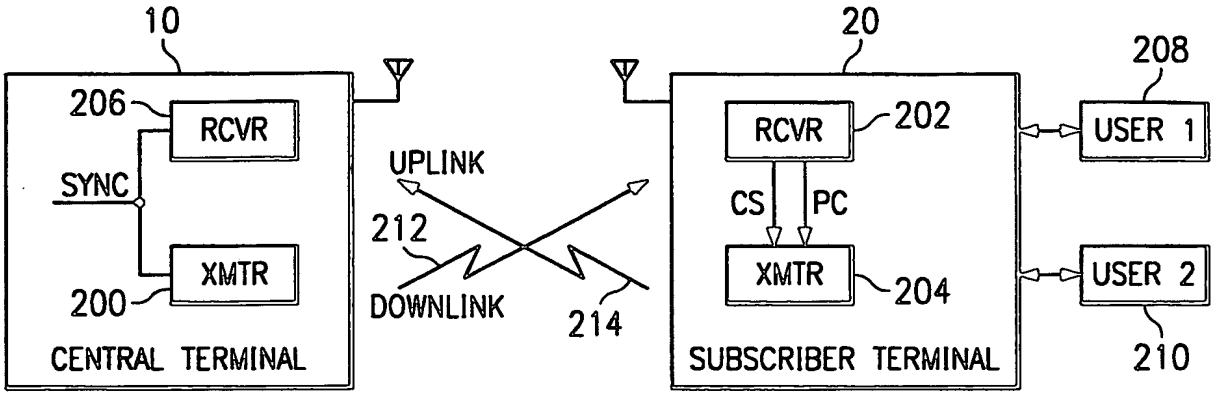


FIG. 9

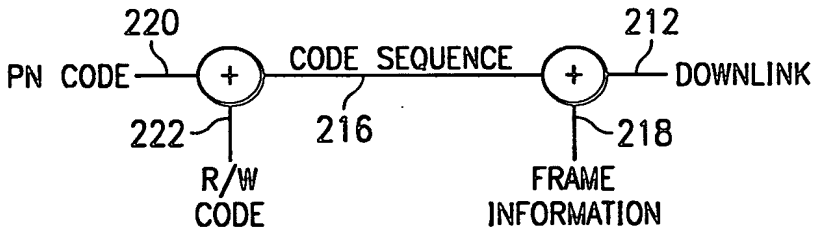


FIG. 10

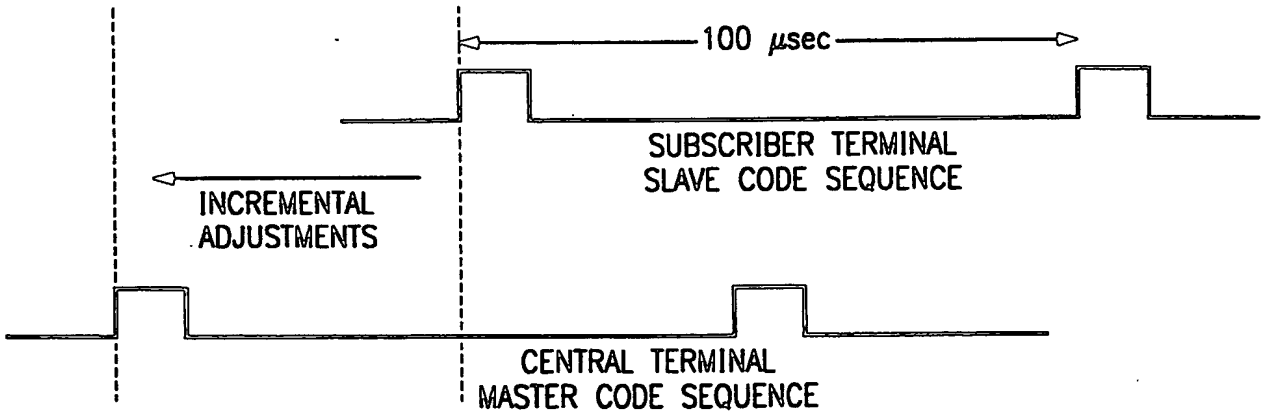


FIG. 11

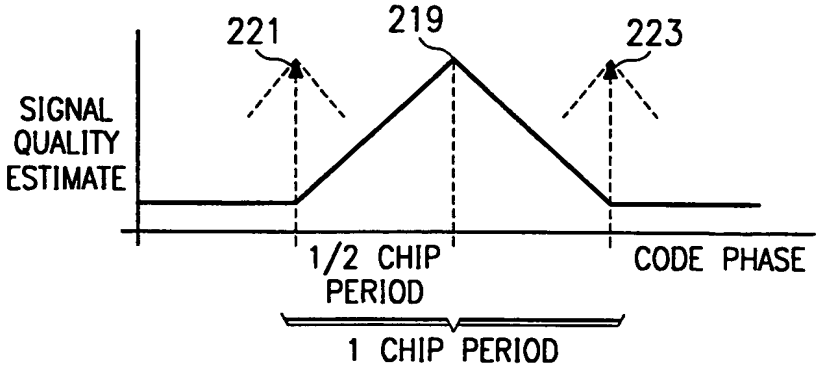


FIG. 12

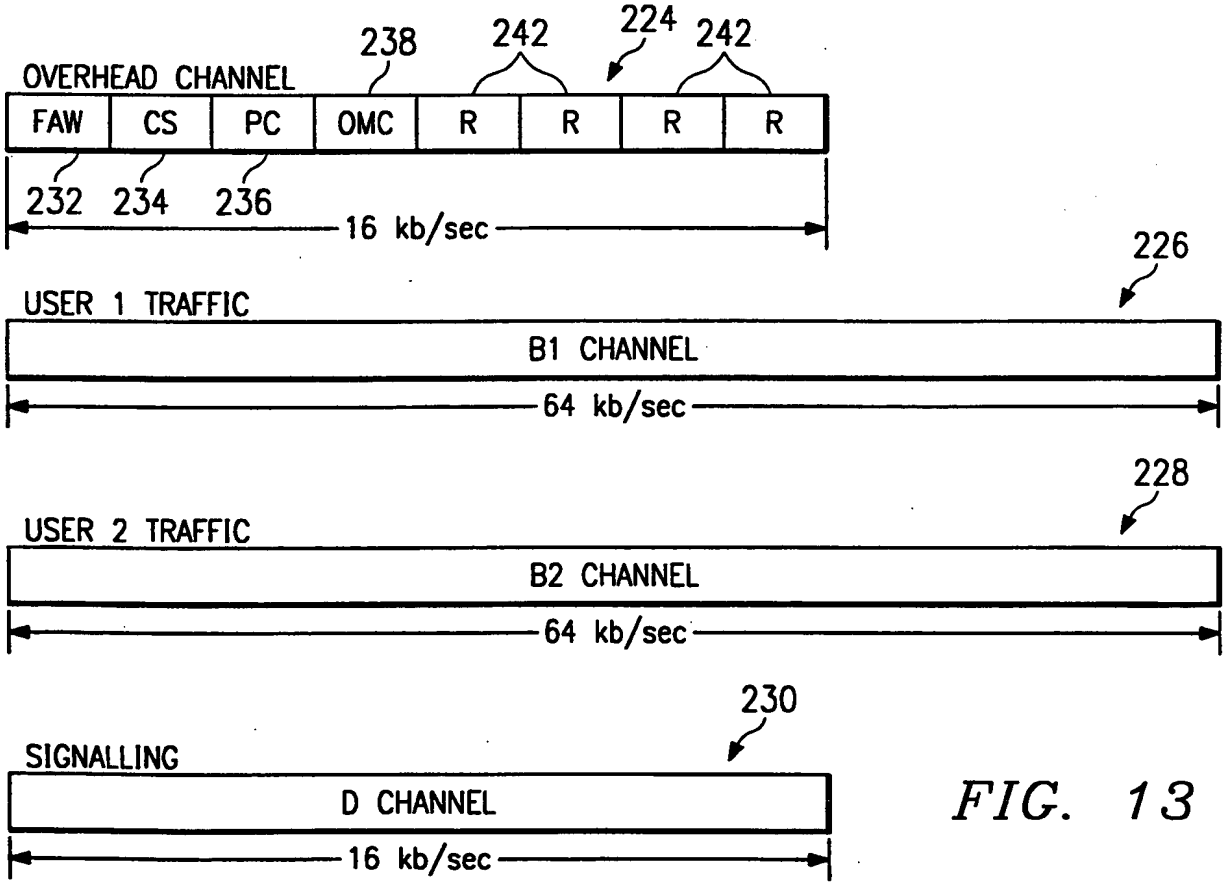


FIG. 13

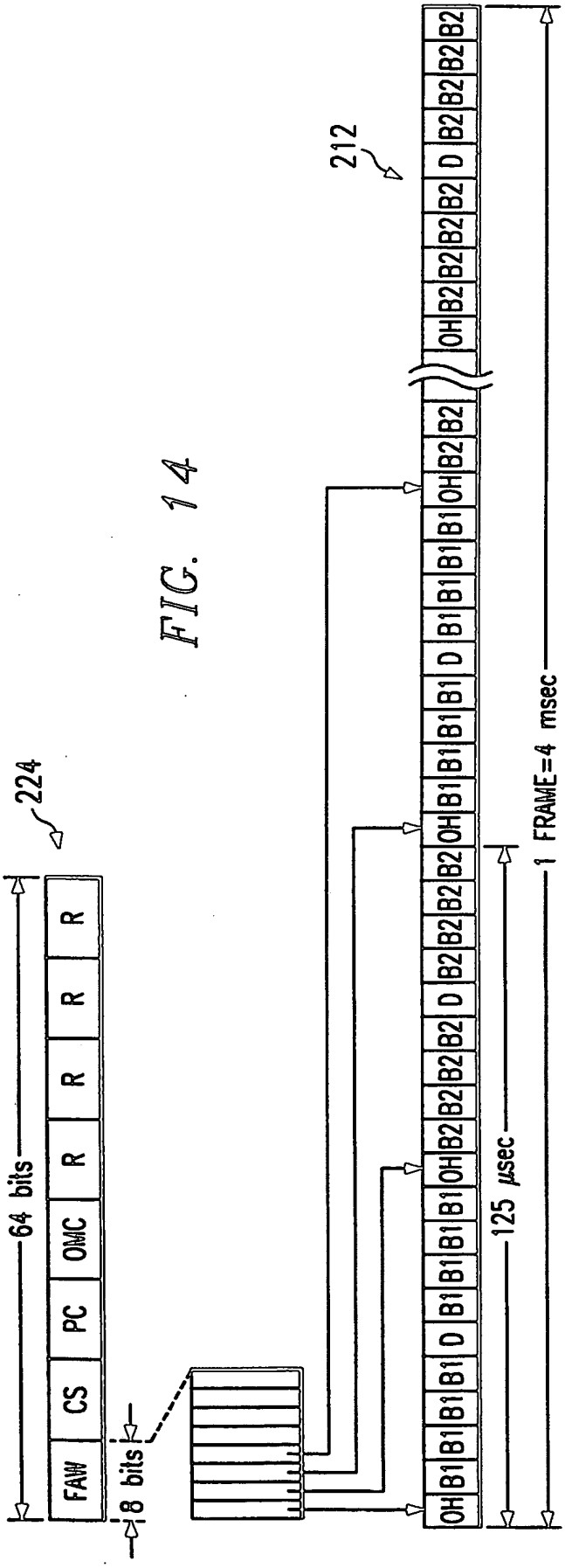


FIG. 14

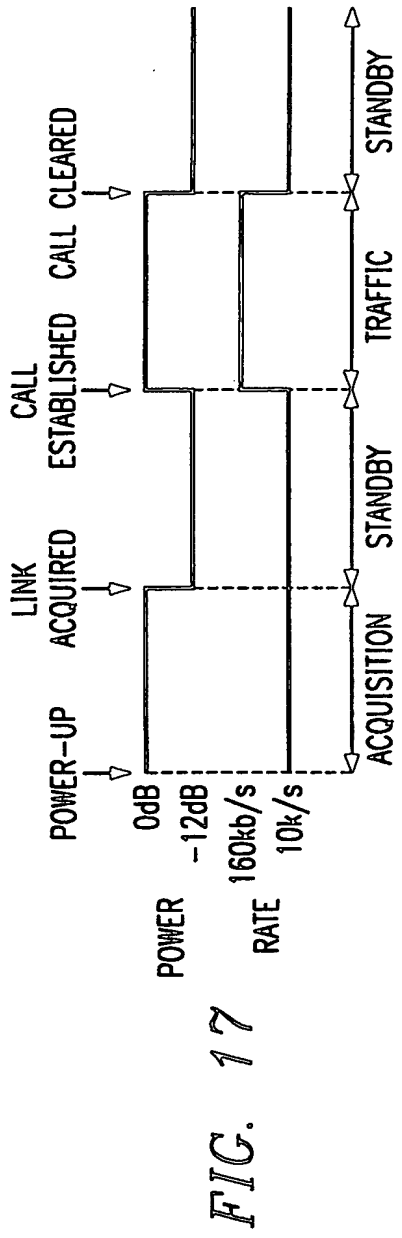


FIG. 17

RLT EPLD–DSP Interface Map

F000 (WR)– PC Control Byte

B7	B6	B5	B4	B3	B2	B1	B0

B7..B0

0C3H	Coarse Power Increment (1dB STEP)	High Rate
0CCH	Coarse Power Decrement (1dB STEP)	High Rate
0C0H	No change	High Rate
0C5H	Fine Power Increment (0.1dB Step)	High Rate
0CAH	Fine Power Decrement (0.1dB Step)	High Rate
063H	Coarse Power Increment (1dB STEP)	Low Rate
06CH	Coarse Power Decrement (1dB STEP)	Low Rate
060H	No change	Low Rate
065H	Fine Power Increment (0.1dB Step)	Low Rate
06AH	Fine Power Decrement (0.1dB Step)	Low Rate
03CH	Reset to minimum power output	
0A5H	set to nominal power mode (using NVRAM value)	

*NOTE: bit reversal takes place at the RNU, to decode the command bit reversed data must be used.

FIG. 15

CS Control Byte

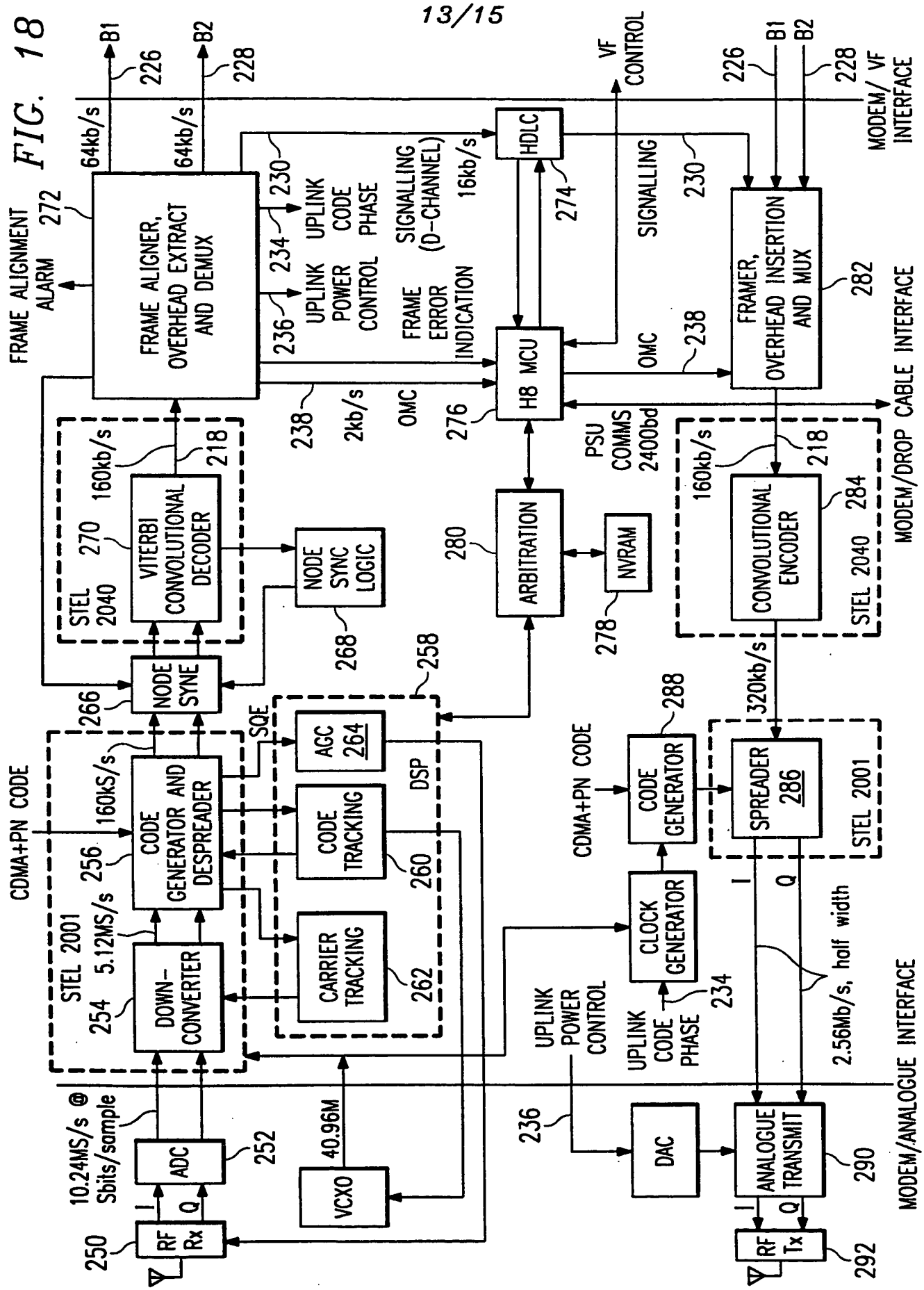
B7	B6	B5	B4	B3	B2	B1	B0

B7..B0

00AH	Fine Advance 1/16 step	High Rate, No Link
005H	Fine Delay 1/16 step	High Rate, No Link
003H	Coarse Advance 1/2 step	High Rate, No Link
00CH	Coarse Delay 1/2 step	High Rate, No Link
000H	No change	High Rate, No Link
006H	Set RNU to AUTO frame mode	High Rate, No Link
00FH	Reset RNU TX EPLD clock chain	High Rate, No Link
02AH	Fine Advance 1/16 step	LOW Rate, No Link
025H	Fine Delay 1/16 step	LOW Rate, No Link
023H	Coarse Advance 1/2 step	LOW Rate, No Link
02CH	Coarse Delay 1/2 step	LOW Rate, No Link
020H	No change	LOW Rate, No Link
026H	Set RNU to AUTO frame mode	LOW Rate, No Link
02FH	Reset RNU TX EPLD clock chain	LOW Rate, No Link
08AH	Fine Advance 1/16 step	High Rate, Link Up
085H	Fine Delay 1/16 step	High Rate, Link Up
083H	Coarse Advance 1/2 step	High Rate, Link Up
08CH	Coarse Delay 1/2 step	High Rate, Link Up
080H	No change	High Rate, Link Up
086H	Set RNU to AUTO frame mode	High Rate, Link Up
08FH	Reset RNU TX EPLD clock chain	High Rate, Link Up

FIG. 16

FIG. 18



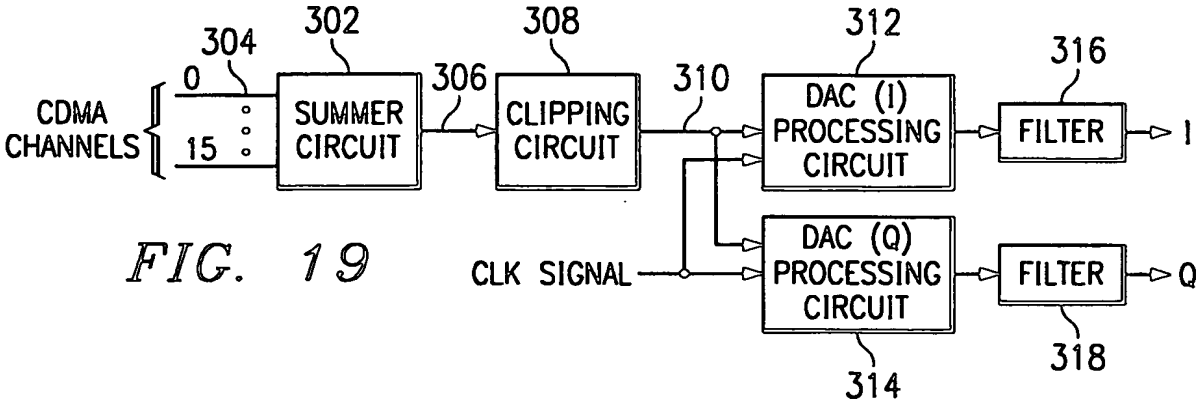


FIG. 19

SUMMED SIGNAL DECIMAL	2'S COMP (8 BITS)	OFFSET BINARY (8 BITS)	CLIPPED SIGNAL DAC DATA (10 BITS)	CLIPPED SIGNAL (HEX DATA)
+64	01000000	11000000		
....	40 hex			
+60	00111100	10111100	11,1111,1111	3FF
....		AO hex		
+32	00100000	10100000		
+31	00011111	10011111	11,1111,1111	3FF
+30	00011110	10011110	11,1110,1111	3EF
....				
+2	00000010	10000010	10,0010,1111	22F
+1	00000001	10000001	10,0001,1111	21F
0	00000000	10000000	10,0000,1111	20F
−1	11111111	01111111	01,1111,1111	1FF
−2	11111110	01111110	01,1110,1111	1EF
....				
−30	11100010	01100010	00,0010,1111	02F
−31	11100001	01100001	00,0001,1111	01F
−32	11100000	01100000		
....	EO hex	60 hex	00,0001,1111	01F
−63	11000001	01000001		
−64	11000000	01000000		
	CO hex	40 hex		

FIG. 20

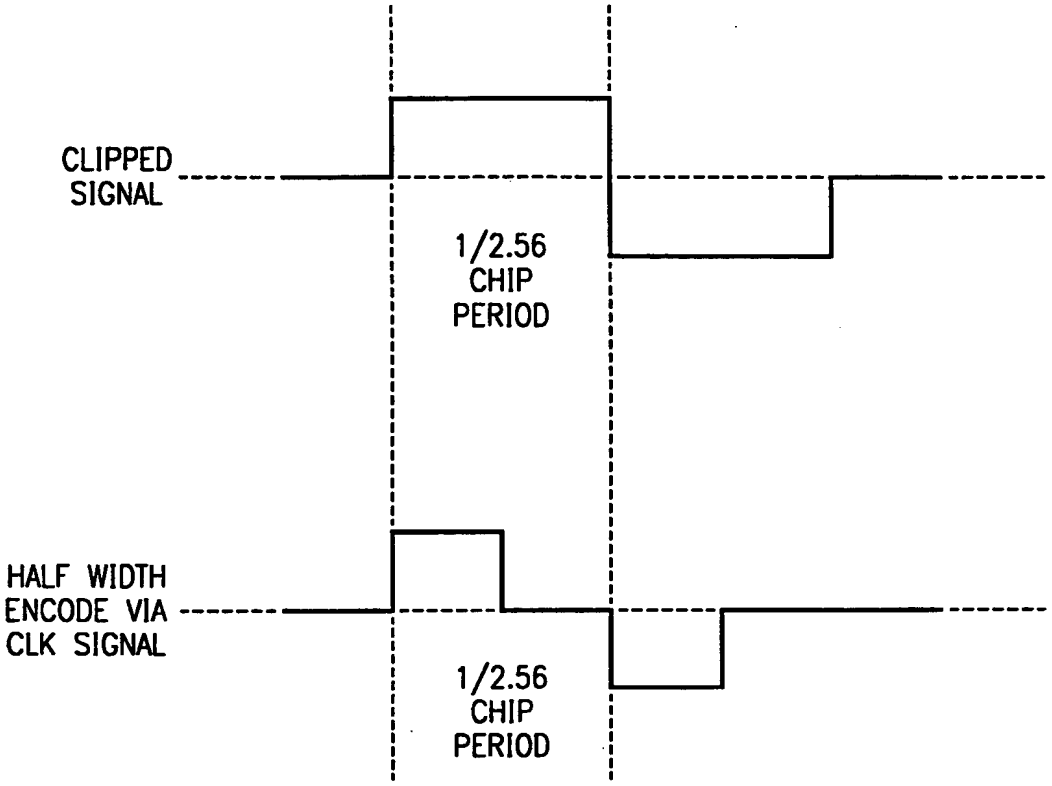


FIG. 21

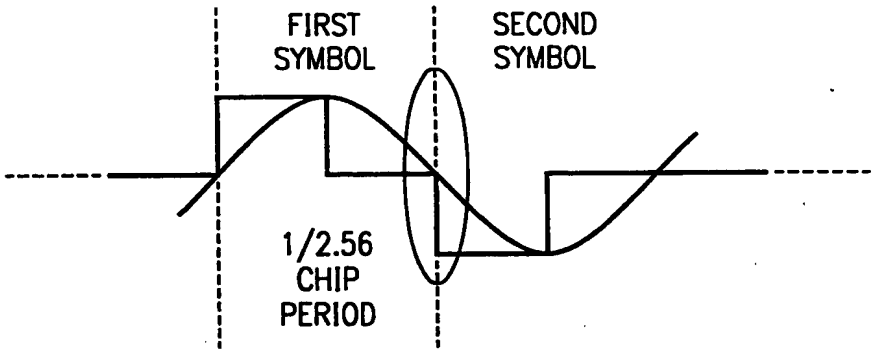


FIG. 22

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 96/08500

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H04J13/04

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H04J H04B H03G

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US,A,5 103 459 (GILHOUSEN KLEIN S ET AL) 7 April 1992 see column 24, line 54 - column 25, line 27; figure 4 ---	1,11,21
X,P	MILCOM 95. UNIVERSAL COMMUNICATIONS. CONFERENCE RECORD , PROCEEDINGS OF MILCOM `95, vol. 3, November 1995, NY, USA, pages 952-956, XP000586663 OZLUTURK F M ; LOMP G : "Effect of limiting the downlink power in CDMA systems with or without forward power control"	1
A	see paragraph 4; figure 1 see paragraph 5 --- -/--	21

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
7 November 1996	18. 11. 96

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+ 31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+ 31-70) 340-3016	Bossen, M

Form PCT/ISA/210 (second sheet) (July 1992)

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US,A,5 216 693 (NAKAMURA M) 1 June 1993 see column 1, line 36 - line 59 see column 2, line 40 - line 65 see column 4, line 38 - line 56; figure 1ABC -----	11

4

INTERNATIONAL SEARCH REPORT

Internal application No.
PCT/US 96/08500

Box I Observations where certain claims were found unsearchable (Continuation of item 1 of first sheet)

This International Search Report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the International Application that do not comply with the prescribed requirements to such an extent that no meaningful International Search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box II Observations where unity of invention is lacking (Continuation of item 2 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

1. claims 1-10,21-24: clipping of a composite CDMA signal at the transmitter
2. claims 11-20: converting a composite CDMA signal into two separate data channels

1. ☒ As all required additional search fees were timely paid by the applicant, this International Search Report covers all searchable claims.

2. ☐ As all searchable claims could be searches without effort justifying an additional fee, this Authority did not invite payment of any additional fee.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this International Search Report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this International Search Report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest.

☒ No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/US 96/08500

Patent document cited in search report	Publication date	Patent family member(s)		Publication date
US-A-5103459	07-04-92	AU-B-	652956	15-09-94
		AU-A-	8401691	23-01-92
		BG-A-	97222	27-05-94
		CA-A-	2085890	26-12-91
		CN-A-	1061312	20-05-92
		EP-A-	0536334	14-04-93
		HU-A-	64657	28-01-94
		IL-A-	98598	27-02-94
		JP-T-	6501349	10-02-94
		SK-A-	387192	10-08-94
		WO-A-	9200639	09-01-92
		US-A-	5511073	23-04-96
		US-A-	5504773	02-04-96
		US-A-	5535239	09-07-96
		US-A-	5568483	22-10-96
		US-A-	5416797	16-05-95
		US-A-	5309474	03-05-94
US-A-5216693	01-06-93	JP-A-	4347943	03-12-92